Electronics
**Digital Electronics**

* Boolean Algebra:* It was developed by George Boole by the help of switches [Relay Circuits].

Boolean Algebra developed three theorems are called Basic Theorem or Boolean Theorem.

1. **NOT Theorem:**

   \[
   \begin{array}{c|c|c}
   \text{1} & \rightarrow & \text{0} \\
   \text{0} & \rightarrow & \text{1} \\
   \overline{A} & \rightarrow & \overline{\overline{A}} = A \\
   \end{array}
   \]

2. **AND Theorem (·):**

   \[
   \begin{array}{c|c|c|c|c}
   0 \cdot 0 & = & 0 & 0 \cdot A & = & 0 \\
   0 \cdot 1 & = & 0 & 1 \cdot A & = & A \\
   1 \cdot 0 & = & 0 & A \cdot A & = & A \\
   1 \cdot 1 & = & 1 & A \cdot \overline{A} & = & 0 \\
   \end{array}
   \]

3. **OR Theorem (+):**

   \[
   \begin{array}{c|c|c|c|c}
   0 + 0 & = & 0 & 0 + A & = & A \\
   0 + 1 & = & 1 & 1 + A & = & 1 \\
   1 + 0 & = & 1 & A + A & = & A \\
   1 + 1 & = & 1 & A + \overline{A} & = & 1 \\
   \end{array}
   \]
Distributive Theorem:

\[ u = (A+B)(A+C) \]
\[ = A \cdot A + A \cdot C + A \cdot B + B \cdot C \]
\[ = A + AC + AB + BC \]
\[ = A [1 + C + B] + BC = A \cdot 1 + BC \]

\[ u = A + BC \]

(*

Short Trick: When two brackets are available and first term of both brackets are same then we apply distributive theorem like this:

\[ u = (A+B)(A+C) \]
\[ u = A \cdot A + B \cdot C \]
\[ u = A + BC \]

(*

Question: For the given expression find the minimise equation.

\[ y = (A+B)(A+B)(A+B)(A+B) \]
\[ y = (A \cdot A + B \cdot B)(A \cdot A + B \cdot B) \]
\[ y = (A+0)(B+0) \]
\[ = A \cdot B = 0 \text{ Ans} \]

Question: For the given expression find the minimise eqn.

\[ y = (A+B+c)(A+B+c)(A+B+c) \]
\[ y = (A + B + C)(A + B + \bar{C})/(A + \bar{B} + C) \]

Let \(A + B = x\).

So,
\[
\begin{align*}
y &= (x + C)(\bar{x} + \bar{C})(A + \bar{B} + C) \\
y &= (x \cdot \bar{x} + C \cdot \bar{C})(A + \bar{B} + C) \\
y &= x(A + \bar{B} + C) \\
y &= (A + B)(A + \bar{B} + C)
\end{align*}
\]

Again let \(B + C = y\).

So,
\[
\begin{align*}
y &= (A + B)(A + y) \\
y &= A \cdot A + B \cdot y \\
y &= A + B[\bar{B} + \bar{C}] \\
y &= A + B\bar{B} + BC
\end{align*}
\]

\[
y = A + BC \quad \text{Ans}
\]

*Short Trick*
\[
\frac{(A + B)(A + C)}{1 + 2.3} = A + BC
\]

\[
A + BC \quad \overset{1.2.3}{=} \quad \frac{(A + B)(A + C)}{1 + 2.3}
\]

\[
(1 + 2.3) = (1 + 2)(1 + 3)
\]

Find the minimise expression of the given eqn.
\[
y = B + B\bar{C}
\]

\[
\begin{align*}
y &= B + \frac{B\bar{C}}{1.2.3} \\
y &= (B + B\bar{C}) = (B + \bar{B})(B + \bar{C}) \\
y &= B\bar{C} \quad \text{Ans}
\end{align*}
\]
**Qns:** Find the minimised equation of the given expression.
\[ y = \overline{ABC} + \overline{ABC} + ABC + ABC \]

**Sol:**
\[
\begin{align*}
y &= \overline{ABC} + \overline{ABC} + ABC + ABC \\
&= \overline{ABC} + \overline{ABC} + AB(C + C) \\
&= \overline{ABC} + \overline{ABC} + AB \{C + C\} \\
&= \overline{ABC} + A \{B + B\}(B + C) \\
&= \overline{ABC} + A (B + C) \\
&= \overline{ABC} + AB + AC \\
&= B(\overline{A}C + A) + AC \\
&= B (\overline{A} + \overline{A}C) + AC \\
&= B (\overline{A} + A)(A + C) + AC \\
&= B (A + C) + AC \\
&= \overline{ABC} + BC + AC \quad \text{Ans}
\end{align*}
\]

**Qns:** Find the minimised expression of the given equation. \[ y = \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC \]

**Sol:**
\[
\begin{align*}
y &= \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC \\
&= \overline{ABC} + \overline{ABC} + BC(\overline{A} + A) \\
&= \overline{ABC} + \overline{ABC} + BC \\
&= \overline{ABC} + B \{C + \overline{A}C\} \\
&= \overline{ABC} + B (C + \overline{A})(C + \overline{C}) \\
&= \overline{ABC} + BC(\overline{A} + A) \\
&= \overline{ABC} + BC + AB \\
&= C (\overline{A}B + B) + AB \\
&= C (B + A) + AB \\
\end{align*}
\]
\[
\begin{align*}
y &= \overline{AC} + BC + AB \quad \text{Ans}
\end{align*}
\]
Sum of Product (SOP) And Product of Sum (POS):

1. Sum of Product (SOP):
   It is used variable output of the digital circuit is high.

   Example:
   \[ \begin{array}{ccc}
   \text{A} & \text{B} & \text{C} \\
   0 & 1 & 0 \\
   1 & 0 & 1 \\
   \end{array} \]
   \[ \begin{array}{ccc}
   \text{D} & \text{E} & \text{F} \\
   1 & 0 & 0 \\
   \end{array} \]

2. Product of Sum (POS):
   It is used variable output of the digital circuit is zero.

   Example:
   \[ \begin{array}{ccc}
   \text{A} & \text{B} & \text{C} \\
   0 & 0 & 0 \\
   0 & 1 & 1 \\
   \end{array} \]
   \[ \begin{array}{ccc}
   \text{D} & \text{E} & \text{F} \\
   0 & 1 & 0 \\
   \end{array} \]

   From the given table, find the output minimise expression by using SOP.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

   So, SOP is written for the high output.
\[
\begin{array}{cc|c}
A & B & Y \\
\hline
0 & 0 & 1 \rightarrow A \overline{B} \\
0 & 1 & 0 \\
1 & 0 & 1 \rightarrow A \overline{B} \\
1 & 1 & 0 \rightarrow AB \\
\end{array}
\]

\[
\begin{align*}
Y_{\text{SOP}} &= (\overline{A} \overline{B}) + (A \overline{B}) + (A \cdot B) \\
&= \overline{B} (\overline{A} + A) + AB \\
&= \overline{B} + AB \\
&= (\overline{B} + B)(\overline{B} + A)
\end{align*}
\]

\[Y_{\text{SOP}} = A + \overline{B} \]  \(\text{(i)}\)

For POS:

Since POS written for the low output.

So,

\[
\begin{array}{cc|c}
A & B & Y \\
\hline
0 & 0 & 1 \\
0 & 1 & 0 \rightarrow A + \overline{B} \\
1 & 0 & 1 \\
1 & 1 & 0
\end{array}
\]

So,

\[Y_{\text{POS}} = A + \overline{B} \]  \(\text{(ii)}\)

from equation \(\text{(i)}\) and \(\text{(ii)}\)

So\(\text{exp} = \text{POS}_{\text{exp}}\)

hence from the given truth table find the minimum expression of output.
\[ \begin{array}{c|cccc} \hline \text{ABC} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 1 \\
1 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 \\
\hline \end{array} \]

\[ y_{sop} = \overline{ABC} + \overline{ABC} \]
\[ y_{sop} = B(\overline{AC} + \overline{A\overline{C}}) \]

*Logical Venn Diagram:*

\[ y_{sop} = \overline{AB} + AB + \overline{AB} \]
\[ = A(\overline{B} + B) + \overline{AB} \]
\[ = A + \overline{AB} \]

From the given diagram find the minimise expression for the shaded region by using SOP.
\[
\begin{align*}
\partial \text{sop} &= (A + B) \\
\text{Ans} &= \text{ } \\
\implies (A + A) &= 1 \\
\end{align*}
\]

**Qus:** From the given diagram, find the output expression for the shaded region by using sop.

**Sol.:**

\[
\rho_{\text{sop}} = A \overline{B} + AB + \overline{A} \overline{B}
\]

\[
= A (\overline{B} + B) + \overline{A} \overline{B}
\]

\[
= A + \overline{A} \overline{B}
\]

\[
= (A + \overline{A}) (A + \overline{B})
\]

\[
\rho_{\text{sop}} = A + \overline{B}
\]

**Qus:** For the given diagram, find the minimise expression.

**Sol.:**

\[
\rho_{\text{sop}} = AB \overline{C} + ABC + ABC + \overline{A} \overline{B} \overline{C}
\]

\[
= AB \overline{C} + ABC + BC (A + \overline{A})
\]
\[ Y_{sop} = AB\overline{C} + A\overline{B}C + BC \]
\[ = ABC + C(B + A\overline{B}) \]
\[ = ABC + C[(B + A)(B + B)] \]
\[ = ABC + BC + AC \]
\[ = B(C + AC) + AC \]
\[ = B[(C + A)(C + C)] + AC \]
\[ Y_{sop} = BC + AB + AC \]  \( \text{Ans} \)

**Qns:** Find the minimise expression for the given diagram.
1. Each term taken from the truth table for implementation of SOP expression is called Minterm. Minterm must include every variable.

2. Each term taken from the truth table for the implementation of POS expression it is called as Maxterm. Maxterm will have +ve sign in between and include every variable.

Mathematical Representation of SOP and POS:

For n variable the value assigned to the maximum number of 1's is given by \(2^n-1\).

**SOP:**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>(Y)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

\[\Sigma m(0, 2, 3)\]

★ \(\Sigma m(0, 2, 3)\) 0\(\overline{1}\) 1\(1\) 0\(1\) 1\(\overline{1}\)

**POS:**

Maxterm = \(\Pi M(1)\)

\(\Pi M(1)\) where \(n\) is the no. of variable (here \(2^n-1\))

\(\Sigma P = \Pi M(1)\) SOP is always equal to POS.
Qns. For the given function \( f(A, B, C) = \Sigma m(0, 2, 3, 6) \), find the equivalent POS.

Soln. Here, number of variable = 3

So, \( 2^3 - 1 = 8 - 1 = 7 \)

Equivalent POS is

\[ \Pi M (1, 4, 5, 7) \]

Ans.

Qns. Find the equivalent POS of \( f(A, B, C, D) = \Sigma m(0, 2, 3, 6, 7, 11, 18) \).

Soln. Here, number of variable = 4

So, \( 2^4 - 1 = 15 \)

Equivalent POS is

\[ \Pi M (1, 4, 5, 8, 9, 10, 12, 14, 15) \]

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Note: Representation of SOP or POS without reducing the number of variable is called Canonical form of representation.

Qns. For the given expression \( f(A, B, C) = A + \overline{B}C \) represents minterm of canonical form of SOP. And Identify no. of minterms present.

Soln. \( f(A, B, C) = A + \overline{B}C \)
\[ f(A, B, C) = A \cdot 1 + \overline{B} \cdot C \cdot 1 \]
\[ = A \overline{(B + \overline{B})(C + \overline{C})} + \overline{B} \cdot C \cdot \overline{A + \overline{A}} \]
\[ = A \overline{B} \cdot C + \overline{B + \overline{B}} \cdot C + \overline{A + \overline{A}} + \overline{B} \cdot C + \overline{A + \overline{A}} \]
\[ = ABC + \overline{A} \overline{B} C + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} C + \overline{A} \overline{B} \overline{C} \]
\[ \text{ Ans, } \]
\[ \text{There is } 8 \text{ minterms.} \]

**IInd Method:**

\[
\begin{array}{ccc}
A & B & C \\
0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 \\
0 & 1 & 0 & 0 \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 0 \\
\end{array}
\]

\[ g_{\text{simp}} = ABC + A\overline{B}C + \overline{A}BC + \overline{ABC} + \overline{ABC} \]

**Ans:**

For the given function find the number of minterms

1. \[ f(A, B, C, D) = A + \overline{C} \overline{D} \]
2. \[ f(A, B, C, D) = B + c \overline{D} \]

**Sol**:

\[ f(A, B, C, D) = A + \overline{C} \overline{D} \]
* Note:

- For a single variable, we have 4 types of truth tables, so we have 4 types of Boolean expression.

  e.g.,

  \[
  \begin{array}{c|cccc}
  A & y_1 & y_2 & y_3 & y_4 \\
  \hline
  0 & 0 & 0 & 0 & 1 \\
  1 & 0 & 1 & 1 & 0 \\
  \end{array}
  \]

\[2^1 = 4\]

- So for \( n \) no. of variables, no. of possible truth table or Boolean expression or switching expression is given by \( 2^{2^n} \)
for 4-variable no of possible boolean expression is given by -

\[ 2^4 = 2^{16} = 2^{10} \times 2^6 = 1024 \times 64 = 65536 \ \text{Ans.} \]

Positive Logic and Negative Logic:

- If higher values are assigned to higher voltages and lower values are assigned to lower voltages such a logic is called +ve logic.
  
  e.g.-
  
  [Diagram showing voltage levels for logic 0 and 1]

- If the values are reverse the resultant logic will be negative logic.
  
  e.g.-
  
  [Diagram showing voltage levels for logic 0 and 1]

The process of conversion of +ve logic to negative logic or vice-versa is called as "duality."

[Table showing truth values for AND and OR operations with corresponding +ve and -ve logic results]
Important Point for duality:

(i) \[ O \longrightarrow 1 \]

(ii) \[ \cdot \longrightarrow + \]

(iii) Variable as it is.

Examples:

\[
\begin{align*}
A \cdot B & \quad \text{duality} \quad \rightarrow \quad A + B \\
A + B & \quad \rightarrow \quad A \cdot B \\
\frac{A}{B} & \quad \rightarrow \quad \frac{A}{B} \\
(A + B) & \quad \rightarrow \quad (A + B) = (A + B) + \frac{A + B}{B} \\
(A + B) & = (A + B) \{ \text{self dual} \}
\end{align*}
\]

Q: Find the dual of \( y = AB + CD \)

S: \[
\begin{align*}
\bar{y} &= (A + B) \cdot (C + D) \\
\bar{y} &= A \cdot B + C \cdot D \\
\end{align*}
\]

Q: Find the dual of \( y = AB + BC + AC \).

S: \[
\begin{align*}
\bar{y} &= (A + B) \cdot (B + C) \cdot (A + C) \\
&= (B + A \cdot C) \cdot (A + C) \\
&= (B + AC) \cdot (A + C) \\
&= A \cdot B + B \cdot C + A \cdot AC + A \cdot CC \\
&= A \cdot B + B \cdot C + A \cdot C + A \cdot C \\
\end{align*}
\]

\( \bar{y} = A \cdot B + B \cdot C + A \cdot C \) \{ self dual \}
If single time dual results some expression then it is called self dual expression.

Find the dual of given expression -

\[ y = (A+B) \cdot (B+C) \cdot (A+C) \]

\[ y_D = AB + Bc + Ac \]  \( \text{(1)} \)

Since eqn (1) is self dual so

\[ y = (A+B) \cdot (B+C) \cdot (A+C) \] is also self dual expression.

Check whether self dual or not?

\[ y = AB + BC + AC \]

\[ y_D = (\overline{A} + B) \cdot (\overline{B} + C) \cdot (\overline{A} + C) \]

\[ = (\overline{B} + \overline{A}) \cdot (\overline{B} + C) \cdot (\overline{A} + C) \]

\[ = (\overline{B} \overline{A} + \overline{A} C) \cdot (\overline{A} + C) \]

\[ = (\overline{B} + \overline{A} C) \cdot (\overline{A} + C) \]

\[ = \overline{A}B + B\overline{C} + \overline{A} \cdot \overline{A} C + \overline{A} \cdot \overline{C} \overline{C} \]

\[ y_D = AB + BC + AC \]

Self dual expression.

Q. \[ y = (A+B) \cdot (B+C) \cdot (A+C) \] check duality.

It's also a self dual.
Current prefers resistance less path.

Note:

Duality of single variable:

\[
\frac{A}{A} \xrightarrow{D} \left( \frac{A}{A} \right) \quad 2^{1-1} = 1^2 = 2^0 = 2^1 = 2 \quad \text{self dual expressions}
\]

For number number of variable number of possible self dual expression is given by:

\[
2^n - 1
\]

\{( \text{Switching Circuits})\}

The circuit produces same input same output condition is called Buffer.

Common collector configuration is also called Buffer.

\[
\begin{array}{c}
\text{closed} = 1 \\
\text{open} = 0
\end{array}
\]

Buffer:

Filament (A type of resistance)

NOT Gate.
Bistable Multivibrator.

Even numbers of NOT gate with feedback is called as bistable multivibrator.

Astable Multivibrator. (Not Stable)

The output waveform of astable multivibrator is square wave.

Odd numbers of NOT gate combination with feedback is called astable multivibrator.

Equivalent Symbols:

\[
\begin{array}{c|c|c}
A & B & y \\
0 & 0 & 0 \\
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 1 \\
\end{array}
\]

AND gate. Invert Condition: if any \(i\) or \(j\) is high, then output is 0.
In an AND gate, switches are in series.

---

**OR Gate**

Equivalent circuit symbols:

\[ \begin{array}{c}
A \\
B
\end{array} \rightarrow y = A + B \]

Rectangular form of representation:

\[ \begin{array}{c}
A \\
B
\end{array} \rightarrow y = 1 \]

Means one or more than one input is 1 then output is 1.

---

**Universal Gates**

* NAND and NOR gates are universal because any digital circuit can be implemented by using these gates.*
NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A·B</th>
<th>\overline{A·B}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>1</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

When any input is zero then output = 1.

* NOR:

Equivalent Circuit Symbol:

Equivalent rectangular representation:
<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>A + B</th>
<th>A + B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

If any \( i/p = 1 \) then \( o/p = 0 \)

For the given switch diagram, find the \( o/p \) minimise boolean expression.

**Solution:**

\[
y = (A + \overline{A}B)(A + \overline{A}B) \\
= (A + B)(A + \overline{B}) \\
= A \cdot A + B \cdot \overline{B} \\
= A + 0 \\
= A \overline{A} \overline{B}
\]

\( o/p \) minimise expression.
contain Bar. But when switches are in parallel with bulb then of contain Bar.

**Q1.** For the given switch diagram find the output expression.

**SOL**

**Q2.** Calculate output $y$ for two different cases for which given circuit shown.

**SOL**

Case I:

\[ A = B = C = D = E = F = G = 1 \]

So, $O/P = 1$

Case II:

\[ A = B = C = D = 0, E = 1, F = G = 0 \]

So, $O/P = 0$
Arithmetic Circuit Gate:

Ex-OR gate and Ex-NOR are arithmetic circuit gates because most of the arithmetic circuits utilize Ex-OR & Ex-NOR operations.

Ex-OR:

- Ex-OR = Exclusive OR = X-OR
- Symbol: +

- Circuit Symbol:

\[ y = A \oplus B = \overline{AB} + AB \]

Equivalent circuit symbol of Rectangular:

\[
\begin{array}{c}
A \\
\hline
B \\
\hline
\end{array}
\]

The disadvantage of XOR gate is only two input XOR operations are possible.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y = \overline{AB} + AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

For same input, output = 0, for different input output = 1.
If one input of X-OR gate is 1, then output is complement of another input.

If any one input is zero then output is another input.

Switching Diagram:

For the given circuit diagram determine the output.

Ans. So \( y = 0 \).
\[
\frac{\overline{A \cdot B}}{A + B} = \overline{A \cdot B} \quad \text{Demorgan theorem.}
\]

Q1: For the given circuit diagram determine \( y \).
(a) \( x \)
(b) \( \overline{x} \)
(c) \( 1 \) [\( \times \)]
(d) \( 0 \)

Q2: For the given circuit diagram calculate \( y \).
(a) \( A \cdot \overline{B} \) [\( \times \)]
(b) \( A \cdot \overline{B} \) [\( \times \)]
(c) \( \overline{A} \cdot \overline{B} \) [\( \times \)]
(d) \( \overline{A} \cdot B \)

<table>
<thead>
<tr>
<th>( A )</th>
<th>( B )</th>
<th>( \overline{A + B} )</th>
<th>( \overline{A \cdot B} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
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<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
**Ex-Or** is also called as **odd function of** \( z \), i.e. whenever **odd numbers of inputs** are **high**, then output \( = 1 \).

\[
\begin{array}{cccc}
A & B & y \\
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]

**Qus:** For the given circuit diagram find \( y = ? \)

**Ans:**

\[
\begin{array}{cccc}
0 & 1 & 0 \\
1 & 0 & 0 \\
1 & 1 & 0 \\
1 & 1 & 1 \\
\end{array}
\]

So \( 0 \text{ OR } y = 1 \) \text{ Ans}
* **Ex-NOR Gate**

Circuit Symbol:

\[ y = A \oplus B \text{ or } \overline{A \oplus B} \]

\[ A \oplus B = \overline{AB} + \overline{A}B \]
\[ = \overline{A}B + \overline{A}B \]
\[ = AB + \overline{A}B \]
\[ = (A + B)(\overline{A} + B) \]
\[ = A\overline{A} + AB + \overline{A}B + \overline{B} \]
\[ \overline{A \oplus B} = A \oplus B \]

Truth Table:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Ex-NOR is also called equality detector.**

It is also called as coincidence circuit or coincidence gate.

* **Switching Circuit**
For the stairs case application, the logic circuit is used for the control of bulb via X-OR (if X-OR is not available then X-NOR).

Universal Gates

<table>
<thead>
<tr>
<th>Gates</th>
<th>NAND</th>
<th>NOR</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="NAND Circuit" /></td>
<td>$\bar{A} = \overline{A}$</td>
<td>$A + \overline{A} = \overline{A}$</td>
</tr>
<tr>
<td><img src="image" alt="NAND Circuit" /></td>
<td>$y = \overline{A}B$</td>
<td>$y = \overline{A}B$</td>
</tr>
<tr>
<td><img src="image" alt="NAND Circuit" /></td>
<td>$y = A + B$</td>
<td>$y = A + B$</td>
</tr>
<tr>
<td><img src="image" alt="XOR Circuit" /></td>
<td>$y = A \oplus B$</td>
<td>$y = A \oplus B$</td>
</tr>
<tr>
<td><img src="image" alt="XOR Circuit" /></td>
<td>$y = A \oplus B$</td>
<td>$y = A \oplus B$</td>
</tr>
</tbody>
</table>
Observe: Implement $Y = AB + CD$ by using minimum number of two input NAND gate.

\[ Y = \overline{AB} \cdot \overline{CD} \]

\[ Y = \overline{A \cdot B} + \overline{C \cdot D} \]

\[ Y = A \cdot B + C \cdot D \]

Observe: Implement $Y = AB + CD + E$

\[ Y = (A \cdot B + C \cdot D) + E \]

\[ Y = X \cdot E = \overline{X} + \overline{E} \]

Observe: Implement $Y = AB + CD + \overline{E}$

\[ Y = X + \overline{E} = AB + CD + \overline{E} \]

\[ Y = X + \overline{E} = AB + CD + \overline{E} \]
**Question:** For the given expression \( y = (A + B) \cdot (C + D) \) by using minimum number of two input NOR gates.

\[ y = (A + B) \cdot (C + D) \]

**Solution:**

\[ y = \overline{(A + B) + \overline{C + D}} = (A + B) \cdot (C + D) \]

**Question:** For the given expression \( y = (A + B) \cdot (C + D) \cdot E \) by using minimum number of two input NOR gates.

**Answer:**

\[ y = (A + B) \cdot (C + D) \cdot E \]

**Question:** Similarly implement \( y = (A + B) \cdot (C + D) \cdot E \).
<table>
<thead>
<tr>
<th>Gates</th>
<th>NAND</th>
<th>NOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>AND</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>OR</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Ex-OR</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>Ex-NOR</td>
<td>5</td>
<td>4</td>
</tr>
</tbody>
</table>

**Gates by using diodes**

![Diode circuit diagram]

For Gate is OR Gate

**Qus. Identify the logic gate**

![Diode circuit diagram]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>D₁</th>
<th>D₂</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>F.B.</td>
<td>F.B.</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>F.B.</td>
<td>R.B.</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>R.B.</td>
<td>F.B.</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>R.B.</td>
<td>R.B.</td>
<td>1</td>
</tr>
</tbody>
</table>

So, Gate is AND gate.
Question:
For the given circuit diagram determine the output expression. 

\[ \text{AB} = X \]

\[ \text{CD} = Y \]

Output expression: \( y = x + y \)

Answer:
For the given circuit diagram shown in figure, the output expression is \( F \) replace every logic gate by using NAND gate, the resultant expression will be:

(a) \( F \)  (b) \( F_D \)  (c) \( \overline{F_D} \)  (d) \( \overline{F} \)

\( F = (A+B). (C+\overline{D}) \)

\( y = \overline{A \cdot B \cdot C \cdot D} \)

\( y = \overline{A \cdot B + C \cdot D} \)  \( \text{self dual.} \)
For the given circuit diagram shown:

\[ y = AB + CD \]

Replace every gate by NOR gate the resultant expression will be:

(a) \( F \)  (b) \( F_D \)  [X]  (c) \( F_D \)  (d) \( F \)

\[ y = \overline{(A+B)} \cdot \overline{(C+D)} \]

\[ = (A+B) \cdot (C+D) \]

\[ = (A+B) \cdot (C+D) \]

Self dual.

23/July/2014

Logic gates by using Transistor

Quiz for the given circuit diagram identify the logic gate
Ans: Here the transistor is replaced by a switch we get -

\[ \text{NOT Gate.} \]

Ques: For the given circuit diagram identify the logic gate.

Ans: For the given circuit diagram identify the gate.
So, NOR gate.

Identify the gate.
Qns: For the given circuit diagram, find the output function $y$. 

\[ y = \overline{AB} \]

Sol: 
\[ y = \overline{AB} \text{ or } \overline{A}B \]

Logic Circuits

Universal gates are used to implement logic circuits, which are further classified into:

1. Combinational Circuits
2. Sequential Circuits

1. Combinational Circuits:

In combinational circuits, there is no feedback present between output and input, hence no memory-like capacity develops. Examples include Half Adder, Full Adder, Half Subtractor, Full Subtractor, Multiplexer, Demultiplexer, Comparator, etc.
2. Sequential Circuits:

In sequential circuits, feedback is present, hence memory capacity develops. 
Examples: Flip-Flop, Bistable Multivibrator, Register, Counter.

* Combinational Circuit:

# Steps for Combinational Circuits design:

(i) Identify the number of input and output lines.
(ii) Develop the Truth table.
(iii) Minimise the expression by using SOP & POS.
(iv) Implement the logic circuit by using universal gate.

* Half Adder:

It is also called as 2-bit addition.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Sum</th>
<th>Carry</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
SOP expression of \( y_1 \) -

\[
y_1(\text{sum}) = \overline{A}B + A\overline{B}
\]

\[
y_1(\text{sum}) = A \oplus B \quad (i)
\]

SOP expression of \( y_2 \) -

\[
y_2(\text{carry}) = A \cdot B \quad (ii)
\]

**Q1** Implement H.A. by using minimum number of two input NAND gate.

**Soln**

\[
A \quad B \\
\overline{A \cdot B} \\
\overline{A} \quad \overline{B} \\
A \oplus B = \text{Sum}
\]

\[
A \cdot B = \text{Carry}
\]

**Q2** Implement H.A. by using minimum number of NOR gate.

**Soln**

\[
A \quad B \\
\overline{A + \overline{A \cdot B}} = \overline{A + B} = A \cdot B
\]

\[
A \oplus B = \text{Sum}
\]

\[
\overline{A + B} = \overline{A} + B = \overline{A} \cdot B
\]
Half Subtractor:

It is also called as two-bit subtraction.

A \rightarrow \text{H.S.} \rightarrow \text{Difference} \rightarrow \text{Borrow}

Implement Truth Table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Difference</th>
<th>Borrow</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

SOP for Difference:

\[ y_{\text{diff}} = \overline{A}B + AB \overline{B} = A \oplus B \]

SOP for Borrow:

\[ y_{\text{borrow}} = \overline{A}B \]

Implement H.S. by using minimum number of NAND Gate:

\[ \overline{\overline{A}B} = (\overline{A} + B) \]

\[ A \overline{B} \]

\[ \overline{\overline{A}B} = A \overline{B} \]
Qns

Implement H.S. by using minimum number of NOR gates.

\[
\frac{A + B}{A \bar{B} = \bar{A} \bar{B}} \\
\bar{A} + \bar{B} = \bar{A} \bar{B}
\]

H.A. / H.S. \[\rightarrow\] NAND / NOR \[\rightarrow\] 5

\[\star\] Comparator \[\text{Single bit}\] :-

Impliment Truth Table :-

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y_1</th>
<th>Y_2</th>
<th>Y_3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

SOP for \[A \geq B\]:

\[Y_1 = A \bar{B} \]

SOP for \[A = B\]:

\[Y_2 = \bar{A} \bar{B} + AB = A \bar{B} \]

SOP for \[A < B\]:

\[Y_3 = \bar{A} \bar{B} \]
Write the expression for 2-bit Comparator.

For $A = B$

\[ \begin{array}{c}
\text{A} \\
\text{\underline{A}_2 \ A_1} \\
\text{\underline{B}_2 \ B_1} \\
\text{B}
\end{array} \]

\[ \text{Like } 1\ 9 \]
\[ \text{Hence } 1 \leq q \leq 9 \]

Analogous,

\[ (A_2 = B_2) \leq (A_1 = B_1) \]
\[ \Rightarrow (A_2 \oplus B_2) \cdot (A_1 \odot B_1) \]

For $A > B$

\[ \begin{array}{c}
\text{A} \\
\text{\underline{A}_2 \ A_1} \\
\text{\underline{B}_2 \ B_1} \\
\text{B}
\end{array} \]

\[ \text{Like } 1\ 9 \text{ or } 2\ 9 \]
\[ 1\ 9 \ 1\ 9 \]

Analogous,

\[ (A_2 \geq B_2) \text{ or } (A_2 = B_2) \leq (A_1 \geq B_1) \]
\[ = (A_2 \cdot B_2) \cdot (A_2 \oplus B_2) - (A_1 \cdot B_1) \]

For $A < B$

\[ \begin{array}{c}
\text{A} \\
\text{\underline{A}_2 \ A_1} \\
\text{\underline{B}_2 \ B_1} \\
\text{B}
\end{array} \]

\[ \text{Like } 1\ 9 \ 1\ 9 \]
\[ 2\ 9 \ 1\ 9 \]
Let's write the expression for 3-bit comparator.

For $A = B$:

$$
\begin{align*}
(A_3, A_2, A_1) & \in \{199, 199, 199\} \\
(A_3, B_2, B_1) & = (A_3 = B_3) \lor (A_2 = B_2) \lor (A_1 = B_1)
\end{align*}
$$

For $A > B$:

$$
\begin{align*}
(A_3, A_2, A_1) & \in \{200, 199, 199\} \\
(A_3, B_2, B_1) & = (A_3 > B_3) \lor (A_3 = B_3) \lor (A_2 > B_2) \lor (A_1 > B_1)
\end{align*}
$$

For $A < B$:

$$
\begin{align*}
(A_3, A_2, A_1) & \in \{197, 197, 107\} \\
(A_3, B_2, B_1) & = A_3 \overline{B_3} + (A_3 \overline{B_3}) \cdot (A_2 \overline{B_2}) + (A_3 \overline{B_3}) \cdot (A_2 \overline{B_2}) \cdot \overline{A_1} \overline{B_1}
\end{align*}
$$
General Expression for n-bit:

\[ A_n A_{n-1} \ldots A_1 \]

\[ B_n B_{n-1} \ldots B_1 \]

For \( A = B \):

\[ (A_n \ominus B_n), (A_{n-1} \ominus B_{n-1}), \ldots, (A_1 \ominus B_1) \]

For \( A > B \):

\[ A_n B_n + (A_n \ominus B_n) \cdot (A_{n-1}, B_{n-1}) + \ldots + (A_n \ominus B_n) \cdot (A_{n-1} \ominus B_{n-1}) \ldots A_1 \bar{B}_1 \]

For \( A \leq B \):-

-
* Full Adder:

Full Adder is called as 3-bit addition.

![F.A. Diagram]

Truth Table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>SUM</th>
<th>CARRY</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>0</td>
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<td>1</td>
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<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

SOP for SUM:

\[
\bar{\text{SUM}} = \overline{A}BC + \overline{A}\overline{B}C + A\overline{B}\overline{C} + ABC
\]

\[
= \overline{A}(BC + \overline{B}C) + A(\overline{B}\overline{C} + BC)
\]

\[
= \overline{A}[(B \oplus C) + A(\overline{B} \oplus C)]
\]

Let \( B \oplus C = X \)

\[
\bar{\text{SUM}} = \overline{A}X + \overline{A}X
\]

\[
= A \oplus X
\]

\[
\text{SUM} = A \oplus B \oplus C
\]
SOP for Carry:

\[ y_{\text{carry}} = \bar{ABC} + \bar{AB}C + ABC + A \bar{BC} \]
\[ = \bar{ABC} + \bar{AB}C + AC(B + \bar{B}) \]
\[ = \bar{ABC} + A(B \bar{C} + \overline{C}) \]
\[ = \bar{ABC} + A(B + C) \]
\[ = \bar{ABC} + AB + AC \]
\[ = B(\bar{AC} + A) + AC \]
\[ = B(A + C) + AC \]
\[ y_{\text{carry}} = AB + BC + AC \]

Qus. Implement full adder by using minimum number of nand gate.

\[ \text{Sum} = A \oplus B \oplus C \]
\[ \text{Carry} = AB + BC + AC \]

\[ (A \oplus B).C \]
Impliment Full Adder by using minimum number of NOR gate.

Note: for three input $\overline{A} + B + C$ is equivalent to $A + B + C$ with respect to output.

Also find the output minimise expression for three input functions if majority number of inputs are high output is assumed.

Solution:

<table>
<thead>
<tr>
<th>$A$</th>
<th>$B$</th>
<th>$C$</th>
<th>$Y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1 \to \overline{A}BC</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1 \to ABC</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1 \to ABC</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1 \to ABC</td>
</tr>
</tbody>
</table>

$Y_{SOP} = \overline{A}BC + \overline{A}BC + \overline{ABC} + ABC$

$= \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC = \overline{A}BC + ABC + ABC$

$= \overline{B}(A + \overline{C}) + AC = \overline{B}(A + C) + AC = ABC + BC + AC$
Ans. For the previous ques. output is high when minority number of inputs are high.

\[ \begin{array}{cccc|c}
A & B & C & Y \\
0 & 0 & 0 & 1 \rightarrow \overline{ABC} \\
0 & 0 & 1 & 1 \rightarrow \overline{ABc} \\
0 & 1 & 0 & 1 \rightarrow \overline{ABC} \\
0 & 1 & 1 & 0 \\
1 & 0 & 0 & 1 \rightarrow \overline{ABc} \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
1 & 1 & 1 & 0 \\
\end{array} \]

\[ \overline{Y}_{sof} = \overline{ABC} + \overline{ABc} + \overline{ABC} + ABC \]
\[ = \overline{AB}(C + C) + \overline{ABc} + ABC \]
\[ = \overline{AB} + \overline{ABC} + ABC \]
\[ = A[\overline{BC} + BC] + ABC \]
\[ = A[\overline{BC} + BC] + ABC \]
\[ = \overline{AB} + \overline{AC} + ABC \]
\[ = \overline{AB} + \overline{AC} + ABC \]
\[ = \overline{AB} + C(A + AB) \]
\[ = \overline{AB} + C(A + B) \]
\[ \overline{Y}_{sof} = \overline{AB} + \overline{AC} + BC \]

Ans.

Ques. Find the SOP minimised expression for output \( y \) is 1 if input is atleast 3 and maximum is 6.

\[ \begin{array}{cccc|c}
A & B & C & Y \\
0 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 \rightarrow 0 \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
\end{array} \]
\[ y_{\text{sep}} = \overline{ABC} + \overline{A} \overline{BC} + \overline{AB} \overline{C} + \overline{A} \overline{B} \overline{C} \]
\[ = \overline{ABC} + \overline{AB} + \overline{A} \overline{BC} \]
\[ = \overline{ABC} + \overline{A} [ \overline{B} + \overline{C} ] \]
\[ = \overline{ABC} + \overline{A} [ \overline{B} + \overline{C} ] \]
\[ y_{\text{sep}} = \overline{ABC} + \overline{AB} + \overline{AC} \]

25 July 2014

* Full Subtractor \(-\) \[3\text{-bit}\] \(-\) Full Subtractor

is called as 3-bit Subtraction.

Symbol:

\[ \begin{array}{ccc}
A & \overline{B} & \overline{C} \\
\overline{A} & \overline{B} & \overline{C} \\
C & \overline{A} & \overline{B} \\
\end{array} \]

Truth Table:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>\overline{A} \overline{B} \overline{C}</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1 \rightarrow \overline{A} \overline{B} \overline{C}</td>
</tr>
<tr>
<td>\overline{A} \overline{B} \overline{C}</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1 \rightarrow \overline{A} \overline{B} \overline{C}</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1 \rightarrow \overline{A} \overline{B} \overline{C}</td>
</tr>
<tr>
<td>\overline{A} \overline{B} \overline{C}</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
For the **Sum Difference**:

\[ y_{\text{sum}} = \overline{A}BC + A\overline{B}C + A\overline{B}C + ABC \]
\[ = \overline{A}(\overline{B}C + BC) + A[\overline{B}C + BC] \]
\[ = \overline{A}(B\oplus C) + A(\overline{B}\oplus C) \]

Let \( B\oplus C = x \)

\[ y_{\text{sum}} = \overline{A}x + A\overline{x} \]
\[ = A \oplus x \]

\[ y_{\text{sum}} = A \oplus B\oplus C \]

For the **Borrow**:

\[ y_{\text{borrow}} = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}C + ABC \]
\[ = \overline{A}\overline{B}C + A\overline{B}C + BC(A + \overline{A}) \]
\[ = \overline{A}\overline{B}C + B(C + \overline{A}C) \]
\[ = \overline{A}\overline{B}C + B(C + \overline{A})(C + \overline{C}) \]
\[ = \overline{A}\overline{B}C + BC + \overline{A}B \]
\[ = \overline{A}((B + \overline{B}C) + BC \]
\[ = \overline{A}(B + \overline{B})(C + \overline{C}) + BC \]
\[ = \overline{A}(B + \overline{B} + C + \overline{C}) + BC \]
\[ = \overline{A}(B + C) + BC \]

\[ y_{\text{borrow}} = \overline{A}B + \overline{A}C + BC \]

**Ans**
Q. Implement full subtractor by using minimum no. of NAND Gates.

Solution:

Full Subtractor by using NAND Gates.

Note:

\[ FA | FS \rightarrow NAND / NOR \rightarrow 9 \]

Qus. Implement full subtractor by using minimum no. of NOR Gates.

Solution:
Multiplexer

A device which selects a single output line from multiple numbers of input lines and display it at output.

The internal structure of mux is a rotary switch (commutator).

It is used for parallel to serial conversion.

It is also called as universal combinational circuit.

Diagram:

Since here 4 input lines, so, $4 = 2^2$ select lines.

So, there are 2 select lines $(A, B)$.

[4 x 1 Mux]

Here two input lines select $D_0$, $D_1$.

So, 2 select line.

[2 x 1 Mux] So here 1 select line.
Similarly for \( N \) inputs:

\[ \begin{array}{c}
D_0 \\
D_1 \\
\vdots \\
D_n \\
\end{array} \quad Y \\
1 \ 2 \ 3 \ \cdots \ \cdots \ n \]

Here numbers of input lines = \( N \)

So

\[ \begin{array}{c}
\sum \quad \text{No. of select line} \\
\quad \text{No. of inputs} \\
\end{array} \]

A device having \( 2^n \) input lines with \( n \) numbers of select line to select single input and display at the output:

\[ N = 2^n \]

\[ \log N = \log 2^n \]

\[ \log N = n \log 2 \]

Since here binary numbers are used so base of logarithm is 2.

\[ \log_2 N = n \log_2 2 \]

\[ \log_2 N = n \quad \text{or} \quad \text{No. of input lines} \]

\[ \log_2 (N) = \text{No. of select lines} \quad \text{since} \quad \log_2 n = 1 \]
2x1 Multiplexer

Diagram:

\[
\begin{array}{c}
\text{A} \\
\text{\overline{A}B} \\
\text{AB} \\
\text{\overline{A}B} \\
\text{AB} \\
\text{Y} \\
\end{array}
\]

\[
\begin{array}{c|c|c}
A & B & Y \\
\hline
\overline{A} & 0 & 0 \\
\overline{A} & 0 & 1 \\
\overline{A} & 1 & 0 \\
\overline{A} & 1 & 1 \\
\hline
\text{Y} = \overline{A}B \cdot 1 + \overline{A}B \cdot 0 + AB \cdot 1 + AB \cdot 0 = \overline{A}B + AB + AB \\
\end{array}
\]

Solve (Actual):

Due to this reason we cannot take 0 off.

\[
\begin{array}{c|c}
A & Y \\
\hline
\overline{A} & 0 \\
\overline{A} & 1 \\
\overline{A} & 1 \\
\overline{A} & 1 \\
\hline
\end{array}
\]

\[
Y = \overline{A}D_0 + AD_1
\]

Implement 2x1 Mux by using logic gates:

\[
Y = \overline{A}D_0 + AD_1
\]
4x1 Multiplexer:

\[ y = \overline{A} \overline{B} D_0 + \overline{A} B D_1 + A \overline{B} D_2 + A B D_3 \]
Minimisation of logic expression by using Mux.

Type I:

Q: Find the output minimise expression for the given Mux circuit.

\[ Y = \overline{A}\overline{B}D_0 + \overline{A}BD_1 + A\overline{B}D_2 + ABD_3 \]

\[ \text{\textbf{SOL}} \]

\[ Y = \overline{A}BC + \overline{A}B\overline{C} + ABC + A\overline{B}C \]

\[ Y = \overline{A}B(\overline{B} + B) + AC(\overline{B} + B) \]

\[ Y = \overline{A}C + AC \]

\[ Y = AB \lor C \]

Q: For the given circuit diagram find the minimise expression.

\[ Y = \overline{A}BD_0 + A\overline{B}D_1 + A\overline{B}D_2 + AB \]
for the given circuit diagram, find minimise expression.

\[
\begin{align*}
y &= \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC \\
y &= \overline{ABC} + \overline{ABC} + AC \\
y &= \overline{ABC} + (\overline{AB} + A)C \\
y &= \overline{ABC} + C(A + B)(A + A) \\
\end{align*}
\]

Thus, find the output expression \( y \).
\[ y_1 = \overline{A}D_0 + AD_1 \]
\[ y_2 = \overline{A}B + AB \]
\[ y_1 = A \oplus B = E \] (seq)

So, \[ y_2 = E \cdot 0 + E \cdot 1 \]

\[ y_2 = \overline{A} \oplus B, 0 + A \oplus B, 1 \]

\[ y_2 = A \oplus B \]

Thus, find the output minimise expression.

\[ \gamma = \overline{A}BC + \overline{A}B \cdot 0 + AB \cdot C + ABC \]
\[ y = \overline{A \overline{B} C} + \overline{A} B (C + \overline{E}) + A \overline{B} \cdot 0 + ABC \]
\[ = \overline{A} B C + A B \cdot 1 + A B C \]
\[ = \overline{A} (B + \overline{B} C) + A B C \]
\[ = \overline{A} (B + C) + A B C \]
\[ = \overline{A} B + \overline{A} C + A B C \]
\[ = \overline{A} B + C \left[ \overline{A} + A B \right] \]
\[ y = \overline{A} B + \overline{A} C + B C \]

**Ans**

- **Type II:**

*Implementation of logic circuits by using Mux.*

**2x1 Mux:**

```
Variable  |
          linear
          |
          |
  |   D0   |
  |   D1   |
  |   Y    |
  |  0\rightarrow p |
  |  input |
```

1. **NOT Gate:**

```
Variable  |
          1
          |
          |
  |   D0   |
  |   D1   |
  |   Y    |
  |   A D0 + A D1 |
```

**NOT Gate**
2. **AND Gate**

\[ y = \overline{A}D_0 + AD_1 \]

3. **OR Gate**

\[ y = \overline{A}D_0 + AD_1 \]

\[ y = A + B = A + \overline{A}B \]

\[ = (A + \overline{A})(A + B) \]

\[ = (A + B) \]

4. **EX-OR Gate**

\[ y = \overline{A}D_0 + AD_1 \]

\[ y = \overline{A}B + AB \]
5. **NAND Gate**

\[ y = \overline{A \cdot D_0 + A \cdot D_1} \]

6. **NOR Gate**

\[ y = \overline{A + B} \]

7. **EX-NOR Gate**

\[ y = A \overline{B} + B \overline{A} \]
**Q:** Implement half adder by using 2x1 Mux.

- **Ans:**
  - Sum = $A \oplus B$
  - Carry = $A \cdot B$

**Ans:** Implement half subtractor by using 2x1 Mux.

- **Ans:**
  - Difference = $A \oplus B$
  - Borrow = $A \cdot B$

**Q:** By using 2x1 Mux implement single bit comparator.

- **Ans:** Single bit comparator has 3 o/p s (for A > B, A = B & A ≤ B). So we use 3 2x1 mux.
2. Construct gate by using 4x1 Mux.

1. AND Gate:
   - \( y = A \cdot B \) for \( A \neq B \)
   - \( y = A \oplus B = \overline{A} \overline{B} + AB \) for \( A = B \)

2. Ex-OR Gate:
   - \( y = \overline{A} \overline{B} + A \overline{B} \)
3. **OR Gate**:

\[ y = \bar{A} B + A \bar{B} + A B = \bar{A} B + A (\bar{B} + B) \]
\[ y = \bar{A} B + A = (\bar{A} + A) (A + \bar{A}) \]
\[ y = A + B \]

4. **NOT Gate**:

5. **Ex-NOR Gate**:

\[ y = A \bar{B} + A B \]
6. NAND Gate:

\[ Y = \overline{A \overline{B}} + \overline{A} B + A \overline{B} = \overline{A(B \overline{B})} + \overline{A} + A \overline{B} = (A + \overline{A})(A + \overline{B}) \]

\[ Y = \overline{A} \overline{B} \]

\[ \therefore A + \overline{A} = 1 \]

\[ \therefore \overline{A + \overline{A}} = \overline{A \overline{B}} \]

7. NOR Gate:

\[ Y = \overline{A \overline{B}} = (A + B) \]

*Type III:*

Identification of number of Mux required for the implementation of higher order Mux by using lower order Mux.

Qns: Implement 4x1 Mux by using 2x1 Mux.

\[
\begin{array}{c}
4x1 \\
4+1=3
\end{array} \rightarrow \begin{array}{c}
2x1 \\
2+1=3
\end{array}
\]

\[
\begin{array}{c}
8x1 \\
4+2+1=7
\end{array} \rightarrow \begin{array}{c}
2x1 \\
2+1=3
\end{array}
\]

\[
\begin{array}{c}
16x1 \\
8+4+2+1=16
\end{array} \rightarrow \begin{array}{c}
2x1 \\
2+1=3
\end{array}
\]
Similarly, \( 2^n \times 1 \rightarrow 2^{n-1} \rightarrow 2^n \times 1 \).

\[ 4 \times 1 \text{ (Mux) } \]

**Qn:** Implement 8x1 Mux by using 4x1 Mux.

**Sol:**
Type - IV

Implementation of higher order function by using lower order Mux.

Qns: Implement \( f(a, b) = \sum m(0, 1, 3) \) by using 4x1 Mux, and 2x1 Mux.

\[ \begin{array}{cccc}
1 & D_0 & D_1 & \downarrow \\
1 & D_2 & D_3 & \downarrow \\
0 & & & Y \\
1 & & & \\
\end{array} \]

For 2x1 Mux:

\[ \begin{array}{cccc}
1 & D_0 & D_1 & \downarrow \\
& & & Y \\
& & & \\
\end{array} \]

Qns: Implement \( f(a, b) = \sum (0, 1, 3) \) by using 2x1 Mux by select line B.
Here value of $A = 0$ so it is 0 no. box in $A$.
Again when $B = 1$ then rotary switch goes to 1.
Then value of $A = 0$ so it will fill in $\overline{A}$ and it is 1 no. box.

**Question**
For the given function $f(a, b, c) = \Sigma m(0, 2, 3, 6, 7)$, implement the function by using 4x1 MUX.

**Solution**

```
<table>
<thead>
<tr>
<th>C</th>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
```

**Note:**
Either substitute 1 in the required box or incircle the desired number is also 1.
Problem: Repeat the previous guess, use \( b, c \) be the select line.

Solution:

\[
\begin{array}{c|c|c|c|c}
\overline{A} & B & C & \rightarrow \overline{0} \\
0 & 0 & 0 & \rightarrow 0 \\
0 & 0 & 1 & \rightarrow 1 \\
0 & 1 & 0 & \rightarrow 2 \\
0 & 1 & 1 & \rightarrow 3 \\
1 & 0 & 0 & \rightarrow 4 \\
1 & 0 & 1 & \rightarrow 5 \\
1 & 1 & 0 & \rightarrow 6 \\
1 & 1 & 1 & \rightarrow 7 \\
\end{array}
\]

Problem: Repeat the same guess, use \( a, c \) be the select line.

Solution:

\[
\begin{array}{c|c|c|c|c}
D_0 & D_1 & D_2 & D_3 \\
0 & 0 & 1 & 0 & \rightarrow 3 \\
0 & 0 & 5 & 6 & \rightarrow 7 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 & \rightarrow 4 \\
1 & 0 & 5 & 7 & \rightarrow 5 \\
1 & 1 & 0 & 1 & \rightarrow 6 \\
1 & 1 & 1 & 1 & \rightarrow 7 \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
A & B & C & \rightarrow \overline{0} \\
1 & 0 & 0 & \rightarrow 0 \\
1 & 0 & 1 & \rightarrow 1 \\
1 & 1 & 0 & \rightarrow 2 \\
1 & 1 & 1 & \rightarrow 3 \\
0 & 0 & 0 & \rightarrow 4 \\
0 & 0 & 1 & \rightarrow 5 \\
0 & 1 & 0 & \rightarrow 6 \\
0 & 1 & 1 & \rightarrow 7 \\
\end{array}
\]
**De-Mux:**

The outer surface of the De-Mux is the mirror image of Mux. The internal structure of De-Mux is equivalent to Decoder.

\[
\begin{align*}
(d_0)_{\text{SOP}} &= \overline{A}D \\
(d_1)_{\text{SOP}} &= \overline{A}D
\end{align*}
\]

Internal Structure of De-Mux contains only AND gate.

\[
1 \times 4 \quad \overset{2+1=3}{\Rightarrow} \quad 1 \times 2 \quad \text{Demux}
\]

\[
1 \times 16 \quad \overset{4+1=5}{\Rightarrow} \quad 1 \times 4
\]
* Decoder *

The I.C. developed for decoder can be used as De-Mux because internal structures are same.

A De-Mux can be exchanged into decoder by interchanging input lines and select line provided the number of input lines should not be equal to number of select lines.

We can't construct 1x2 De-Mux because in 1x2 DeMux no. of input lines = no. of select line.

Therefore the lowest possible decoder is 2x4 decoder.
\[ \text{Implemment half adder by using 2x4 Decoder} \]

\[ \text{Sol} \]

\[ \text{Sum} = A \oplus B = \overline{A} \overline{B} + AB \]

\[ \text{Carry} = A \cdot B \]

\[ \text{By using 2x4 decoder, implement single bit comparator.} \]
By using 2x4 decoder implement the function \( f(A,B) = \sum m(0,1,3) \).

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1 → \overline{A} \overline{B}</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1 → \overline{A} B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1 → A B</td>
</tr>
</tbody>
</table>

\[ Y_{SOP} = \overline{A} \overline{B} + \overline{A} B + A B \]

**Note:** Decoder is non-universal because external gates are used.

*Order of Decoder:*

- Mux: \( 4 \times 1 \)
- Demux: \( 1 \times 4 \)
- Decoder: \( 2 \times 4 = 2 \times 2^2 \)
- Mux: \( 8 \times 1 \)
- Demux: \( 1 \times 8 \)
- Decoder: \( 3 \times 8 = 2 \times 2^3 \)
- Mux: \( n \times 1 \)
- Demux: \( 1 \times n \)
- Decoder: \( n \times 2^n \)

(order of decoders)
Qns. Implement full adder by using 3x8 decoder.

Sol.  

\[ y_{\text{carry}} = AB + B \overline{C} + \overline{A} \overline{B} \overline{C} = \overline{A}BC + \overline{A}BC + \overline{A}BC + \overline{A}BC \]

Full Subtractor
\[ y_{\text{diff}} = A \oplus B \overline{C} = \overline{A}BC + A \overline{B} \overline{C} + \overline{A}BC + A \overline{B} \overline{C} \]
\[ y_{\text{borrow}} = A \overline{B} + \overline{A}C + B \overline{C} = \overline{A}BC + \overline{A}BC + \overline{A}BC + A \overline{B} \overline{C} + A \overline{B} \overline{C} \]

Qns. Implement full subtractor by using 3x8 decoder.

Sol.  

<table>
<thead>
<tr>
<th>A</th>
<th>3x8 Decoder</th>
</tr>
</thead>
<tbody>
<tr>
<td>y_0 = 000</td>
<td>y_1 = 001</td>
</tr>
<tr>
<td>y_2 = 010</td>
<td>y_3 = 011</td>
</tr>
<tr>
<td>y_4 = 100</td>
<td>y_5 = 101</td>
</tr>
<tr>
<td>y_6 = 110</td>
<td>y_7 = 111</td>
</tr>
</tbody>
</table>

\( E = 1 \)

\( E = 1 \)
Codes

Gray Code:
- The outer boundary of K-map is designed on the basis of Gray Code.
- It is called unweighted code.

Weighted Code:
- If each and every bit is having significant positional value then such code is called as weighted code.
  - Ex. 0842
    05211
    03321

If each and every bit does not have significant positions such codes are called as unweighted code.
- Ex. Gray Code, Excess-3 code.

- Gray Code is also called as unit distance code.
- Gray Code is also called as cyclic code.

* Basic formation of Gray Code:

\[ B_3 \quad B_2 \quad B_1 \quad B_0 \]
\[ C_n^3 \quad C_n^2 \quad C_n^1 \quad C_n^0 \]
In the binary to gray conversion, M.S.B. written as it is and side by side, ex-or operation is performed (sum is taken, carry is discarded)

\[ b_3 \ b_2 \ b_1 \ b_0 \quad g_3 \ g_2 \ g_1 \ g_0 \]

\[
\begin{align*}
0 & \oplus 0 \oplus 0 \oplus 0 &= 0 \\
0 & \oplus 0 \oplus 0 \oplus 1 &= 0 \\
0 & \oplus 0 \oplus 1 \oplus 0 &= 0 \\
0 & \oplus 0 \oplus 1 \oplus 1 &= 0
\end{align*}
\]

1-bit difference so it is unit disc code.

**Circuit Diagram:**

- For n-bit binary to gray conversion, the number of ex-or gate will be \((n-1)\).
- Ex-or follow cyclic property.
  - \( A \oplus B = C \)
  - For ex-or follow cyclic property,
    \[
    \begin{align*}
    A \oplus 0 &= C \\
    0 \oplus 1 &= A \\
    A \oplus 1 &= C
    \end{align*}
    \]
    So ex-or follow cyclic property
Karnaugh Map or K-Map?

It is also called as graphical representation of Boolean expression.

The disadvantage of Boolean Algebra (SOF or POS) is, it is applicable for 1 or 0 but K-map is applicable for 1 or 0 or X (don't care)

- K-map is applicable for 2-variable, 3-variable & 4-variable.

1. 2-Variable:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

2. 3-Variable:

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>000</th>
<th>001</th>
<th>010</th>
<th>011</th>
<th>100</th>
<th>101</th>
<th>110</th>
<th>111</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>2</td>
<td></td>
<td></td>
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<tr>
<td>1</td>
<td>0</td>
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<td>2</td>
<td>0</td>
<td>1</td>
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<td>0</td>
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<td>4</td>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>0</td>
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<td></td>
</tr>
<tr>
<td>6</td>
<td>1</td>
<td>1</td>
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<td></td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
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<td></td>
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</tr>
</tbody>
</table>
Grouping of K-Map:

Maximum size of grouping in the k-map will have maximum priority.

In case of grouping, the relation used is $2^n$, where $n$ represents integers.

\[
\begin{align*}
2^n & \quad n = 0, 2^0 = 1 \quad \text{[individual]} \\
n = 1 & \quad 2^1 = 2 \quad \text{[pair]} \\
n = 2 & \quad 2^2 = 4 \quad \text{[quad]} \\
\text{[Maximum priority]} & \quad n = 3, 2^3 = 8 \quad \text{[Oct]}
\end{align*}
\]

E.g.:

[Diagram of invalid grouping]

* In case of k-map diagonal grouping is invalid.
End grouping.

End grouping is valid in k-map.

Note: In the k-map grouping the used value can be used repeated no. of times provided the condition is that the no. of groups should not exceed equal to previous.

2(qn) For the given function \( f(A, B) = \sum m (0, 1, 3) \) find the minimise expression.

\[
\begin{array}{c|c|c}
A & B & \bar{A} + \bar{B} \\
0 & 0 & 1 \\
0 & 1 & 0 \\
1 & 0 & 1 \\
1 & 1 & 0
\end{array}
\]

\[
y = \overline{A} + \overline{B}
\]

\[
(A + A) (A + B)
\]

\[
y = \overline{A} + \overline{B}
\]

2(qn) For the given function \( f(A, B, C) = \sum m (0, 1, 3, 5) \) find the minimise expression.

\[
\begin{array}{c|c|c|c|c|c|c|c|c|c}
A & B & C & \overline{B} & \overline{C} & \overline{A} & \overline{B} & \overline{C} & \overline{A} \\
0 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0
\end{array}
\]

\[
y = \overline{A} \overline{B} + \overline{C} + \overline{A} C
\]
Ques. For the given k-map find the output minimise expression.

\[ a \quad b \quad c \quad 00 \quad 01 \quad 11 \quad 10 \]

\[
\begin{array}{ccc}
0 & 1 & 1 \\
1 & 1 & 1
\end{array}
\]

\[ y = \bar{A} \bar{B} + C \]

Ques. For the given k-map find the output minimise expression.

\[ a \quad b \quad c \quad 00 \quad 01 \quad 11 \quad 10 \]

\[
\begin{array}{ccc}
0 & 1 & 1 \\
1 & 0 & 1
\end{array}
\]

\[ y = 1 \]

If all boxes contain 1 then \( y = 1 \).
If all boxes contain 0 then \( y = 0 \).
If all boxes contain \( X \) then \( y = X \).

Ques. For the given k-map find the output minimise expression.

\[ a \quad b \quad c \quad 00 \quad 01 \quad 11 \quad 10 \]

\[
\begin{array}{ccc}
0 & 1 & 1 \\
1 & 1 & 1
\end{array}
\]

\[ y = \bar{A} \bar{B} + AC \]

Ques. For the given k-map find the minimise expression.
\[ y = \overline{wx} + \overline{wyz} + \overline{wxy} + \overline{wxy} \]

**Qus.** Find the minimisation expression.

**Sol.**

\[ y = \overline{CD} + \overline{AC} + \overline{BC} \]

**Qus.** Find the minimal expression.

**Sol.**

\[ y = \overline{AB} + C + AB \]
Don't Care Condition: \([d, x, \phi]\)

It is mainly used in counter design. By using don't care the number of universal gate required reduces drastically.

Don't care can be assumed as 1 or 0 based on the requirement.

\[
\begin{array}{c|cc}
A & B & 0 \\
\hline
0 & 1 & X \\
1 & 1 & 1 \\
\end{array}
\]

\[
\begin{array}{c|cc}
\bar{A} & B & 0 \\
\hline
0 & 1 & 1 \\
1 & 1 & 1 \\
\end{array}
\]

\[I = \overline{A}B + AB\]  \hspace{1cm} \[Y = \overline{A} + B\]

(max no. of gates required)  \hspace{1cm} \text{(min no. of gates required)}

\[
\begin{array}{c|cc|c|c}
A & B & \overline{A} \odot B & \overline{A} + B \\
\hline
0 & 0 & 1 & 1 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 0 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

**Question:** For the given K-map, find the minimized expression.

**Solution:**

\[
\begin{array}{c|cc|c|c}
0 & 0 & 0 & 0 & 0 \\
0 & 1 & 1 & X & 1 \\
1 & X & 0 & 1 & 1 \\
\end{array}
\]

\[Y = AB + \overline{AB}\]
**Ques** for the given k-map find the minimise expression.

**Sol**

\[
Y = \overline{A} \overline{B} \overline{C} + ABC + \overline{B} \overline{A} \overline{D}
\]

**Ques** for the given k-map find the minimise expression.

**Sol**

\[
Y = C + \overline{A} \overline{B} + AB
\]

**Ques** for the given k-map find the minimise expression.

\[
Y_1 = \overline{B} \overline{C} + AC + \overline{A} \overline{B} \quad Y_2 = BC + \overline{A} \overline{C} + AB
\]
Implicant

Prime Implicant

Essential prime Implicant

for those k-map which produces multiple type of answers.

1. Implicant:

It represents number of minterms or no. of 1's present in the k-map.

2. Prime Implicant:

It is a product term formed by a maximum possible grouping without failing priority. And also include redundant group.

3. Essential prime Implicant:

It is the part of prime implicant but excluded redundant group or if a single k-map produce multiple type of answers then the final one is compare, the no. of common terms present in the final answer represent essential prime implicant.

Any Find Implicant, Prime Implicant and Essential prime Implicant for a given k-map.
\( I = 4 \)
\( P.I = 3 \)
\( E.P.I = 2 \)

\( I = 8 \)
\( P.I = 4 \)
\( E.P.I = 8 \)

**Ques** Find out the parameters \( I, P.I, E.P.I \). 

**Sol**

\( y_1 = \overline{BC} + AC + \overline{A}B \)

\( I = 6 \)
\( P.I = 6 \)
\( E.P.I = 0 \)

\( y_2 = BC + \overline{AC} + A\overline{B} \)

\( y_3 = \overline{BC} + AC + \overline{A}B \)

\( y_4 = BC + \overline{AC} + A\overline{B} \)

\( \text{**Note**: Here no common term in final ans.} \)

**Ques** Find the parameters \( I, P.I, E.P.I \).
\[
\begin{array}{|c|c|c|}
\hline
1 & 1 & 1 \\
\hline
1 & 1 & 1 \\
\hline
\end{array}
\]

\[
J = 5 \\
PJ = 2 \\
EPI = 2
\]

**Q:** For the given function \( f(A, B, C) = \Pi M(2, 4, 6, 7) \), find the k-map

**Ans:**

\[
f(A, B, C, D) = \Pi M(2, 3, 6, 7, 10, 11, 12, 14) = \Sigma m(0, 1, 4, 5, 8, 9, 13, 15)
\]

**Q:** For the given k-map

\[
\begin{array}{c}
A \\
\hline
B \\
\hline
C \\
\hline
D
\end{array}
\]

\[
\begin{array}{|c|c|c|c|}
\hline
1 & 1 & 1 & 1 \\
\hline
1 & 1 & 1 & 1 \\
\hline
\end{array}
\]
Sequential Circuit

Flip-Flop: This is the basic memory element in the digital system. The basic flip-flop is also called Bistable multivibrator. It is a single bit storage device, i.e., it can store either 1 or 0.

A flip-flop can store indefinitely unless and until the input conditions are changed.

Every flip-flop will have two output both will be complement of each other.

Every flip-flop will have cross-coupling in between input and output.
Types of Flip-Flop

1. Latch
2. S-R Flip-Flop
3. J-K Flip-Flop
4. D-Flip-Flop
5. T-Flip-Flop

* Difference between Latch and Flip-Flop:

* Replace every not gate by using NAND gate.

Truth Table:

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1 0</td>
</tr>
</tbody>
</table>

S-R Latch

Complementary S-R Latch:

Replace every NAND gate by NOR gate and interchange either the position of S-R or Q and Q'

Complementary S-R Latch:
**Truth Table**

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Previous Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>invalid</td>
<td></td>
</tr>
</tbody>
</table>

**S-R Flip-Flop**

**Qn** Find the output \( Q \) for the given circuit.

**Solution**

S-R Flip-Flop
Truth Table:

<table>
<thead>
<tr>
<th>X</th>
<th>S</th>
<th>R</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Previous state</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Previous state</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Invalid</td>
</tr>
</tbody>
</table>

The disadvantage of $S\bar{R}$-flip Flop is when $S=R=1$ produces invalid output, can't be use for practical applications.

Flip Flop

Characteristic Table

Characteristic Table

Exitation Table

Characteristic Table

<table>
<thead>
<tr>
<th>0</th>
<th>0</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$Q_{Anti}$</td>
</tr>
</tbody>
</table>

Previous $Q$

Next $Q$
Table \{ Truth Table \}:

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q_n</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>x</td>
</tr>
</tbody>
</table>

Characteristic Equation:

\[ Q_{n+1} = S + \overline{R} Q_n \] \( \text{\{remember\}} \)

Excitation Table:

<table>
<thead>
<tr>
<th>Q_n</th>
<th>Q_{n+1}</th>
<th>S</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>
* State Transition Diagrams :

* The Disadvantage of S-R flip-flop is when $S = R = 1$ produces invalid output. Hence, replaced by J-K Flip-Flop.

* JK-Flip Flop :
* Truth Table *

<table>
<thead>
<tr>
<th>X</th>
<th>J</th>
<th>K</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>P̅</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>P</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

* Characteristic Table *

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>Q_n</th>
<th>Q_{n+1}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

* Characteristic Equation *

\[ Q_{n+1} = J \overline{Q_n} + K Q_n \]

Remember this.
Draw the excitation table of Jk-Flip-Flop:

<table>
<thead>
<tr>
<th>Qn</th>
<th>Qn+1</th>
<th>J</th>
<th>k</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>x</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: Jk-Flip-Flop is also called as universal Flip-Flop.

Rectangular box of J-K Flip-Flop:

- \( x \rightarrow \text{Clk works when } x=1 \)
- \( x \rightarrow \text{does not work } x=0 \)

Meaning of \( x \): Clock which carry on the J-k Flip-Flop.

Edge triggered Clock pulse

Level triggered Clock pulse.
Output changes continuously under the clock pulse as input changes.

In the edge trigger clock pulse output will change either raising edge or falling edge, not both.

\[ \text{Clock (for 1ms)} \]
\[ \text{1ns} \]
\[ \text{Q} \]
\[ \overline{Q} \]

\[ \text{1ms} \]
\[ \text{Raise Around Condition} \]

In the level triggered JK flip-flop output changes many times under a single clock pulse for \( JK = 1 \) it is called as Race Around Condition.

Race around condition is the disadvantage of JK flip-flop.

* Removal of Race Around Condition:
Race around condition can be removed by using edge triggered clock pulse in place of level triggered clock pulse.

Race around condition can be removed by revering the condition $t_{pd\text{ clk}} > t_{pol\text{ ff}}$ to $t_{pd\text{ clk}} < t_{pol\text{ ff}}$. 
To increase the time period of flip-flop, cascading of flip-flop is performed for example. Master slave flip-flop is also useful for race around condition.

* D-Flip Flop:

Truth Table:

<table>
<thead>
<tr>
<th>X</th>
<th>D</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Previous

Characteristic Table:

<table>
<thead>
<tr>
<th>D</th>
<th>Q₀</th>
<th>Q₀+₁</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Characteristic Equation:

\[ Q₀+₁ = D \]

D - flip-flop acts as a buffer.

D - flip-flop is useful for implementation of registers.
\[ = \sum \bar{Q}_n + K Q_n = D \]

Excitation Table:

<table>
<thead>
<tr>
<th>( \bar{Q}_n )</th>
<th>( Q_{n+1} )</th>
<th>( D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

* T-Flip-Flop

Truth Table:

<table>
<thead>
<tr>
<th>( X )</th>
<th>( T )</th>
<th>( \bar{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>( X )</td>
<td>Previous State</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Previous State</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>( \bar{Q} )</td>
</tr>
</tbody>
</table>

Characteristic Table:

<table>
<thead>
<tr>
<th>( T )</th>
<th>( \bar{Q}_n )</th>
<th>( Q_{n+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Previous (0)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Characteristic Equation:

\[ Q_{n+1} = T \oplus Q_n \]

Excitation Table:

<table>
<thead>
<tr>
<th>( Q )</th>
<th>( Q_n+1 )</th>
<th>( T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

T-Flip Flop performs EX-OR operation.

* Point To be Remember:

Characteristic Eqn:

1. SR \( Q_{n+1} = S \bar{R} Q_n \)
2. JK \( Q_{n+1} = J Q_n + K Q_n \)
3. D \( \bar{Q}_{n+1} = D \)
4. T \( Q_{n+1} = T \oplus Q_n \)
**Transition Table**

<table>
<thead>
<tr>
<th>$Q_n$</th>
<th>$Q_{n+1}$</th>
<th>$S$</th>
<th>$R$</th>
<th>$J$</th>
<th>$K$</th>
<th>$D$</th>
<th>$T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

For $X = 1$

<table>
<thead>
<tr>
<th>$J$</th>
<th>$K$</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Previous</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$\overline{Q}$</td>
</tr>
</tbody>
</table>

For $X = 1$

<table>
<thead>
<tr>
<th>$S$</th>
<th>$R$</th>
<th>$Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Previous</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$X$</td>
</tr>
</tbody>
</table>
**Registers**

Mainly implemented by D flip-flop,

To store a number of bits, n flip-flops are required because one flip-flop stores only 1 bit either 0 or 1.

Based on input and output, registers are classified as:

1. **Serial input Serial output Register (SISO)**
2. **Serial input Parallel output Register (SIPO)**
3. **Parallel input Parallel output Register (PIPO)**
4. **Parallel input Serial output Register (PISO)**

1. **Serial input Serial output Register (SISO)**?

   ![Diagram of SISO register]

   1. **D1**
   2. **D2**
   3. **D3**
   4. **Output**

   ![Clock pulse diagram]

   **Clock (t)**

   ![Pulse at t0, t1, t2, t3, t4]
For n bit serial register for input storage n-clock pulse are required.

Qn: For the given circuit diagram, identify the content after three clock pulse.

\[ \text{This is the content after three } \text{CLK} \text{ pulses.} \]
Question: For the given circuit diagram, find the content after 333 clock pulse.

Diagram:

Answer:

1) 1 → 0
2) 1 → 1
3) 0 → 0 → 1
4) 0 → 0 → 0

So after 333 clk pulse we find 0 0 1 2
there for it mean previous state
so after 333 clk pulse we find 10 as
first clk.

For the given circuit find the content after
332 clk pulse.
It is like a not gate.

So after two step we reach previous state.
So after 232 clk we get 001.

Find the content after 3 clock pulse.

So:

Ans
Q1: For the given circuit diagram, identify for which of the following combination of inputs produces high output.

\[
y = 1
\]

\[
A_3 A_2 A_1 A_0 \quad B_3 B_2 B_1 B_0
\]

(a) 1 0 1 0, 1 0 1 0
(b) 0 1 0 1, 0 1 0 1
(c) 0 0 1 1, 0 0 1 1
(d) 0 1 0 1, 0 1 1 1 [Mark]

Q2: For the given circuit diagram, determine the content after 3 clock pulse.

Soln:
$X = A \oplus B$
Counters:

These are used to count the number of clock pulses.
These are used to measure the width (time period) of the clock pulse.
These are used to measure the frequency of clock pulse.
These are used in biomedical application (ECG).
These are used in the radar application.
These are used in the timer' circuit.

Counters are basically classified as:

1. Asynchronous Counter [Slow]
2. Synchronous Counter [Fast]

Classification between Asynchronous and Synchronous Counter:

<table>
<thead>
<tr>
<th>Asynchronous</th>
<th>Synchronous</th>
</tr>
</thead>
<tbody>
<tr>
<td>In the asynchronous counter only one flip-flop is applied by external clock pulse. Rest, every flip-flop receiving clock pulse applied by previous FF.</td>
<td>All the flip-flops are applied by same clock pulse</td>
</tr>
<tr>
<td>Delay is present (Slow)</td>
<td>Delay is not present (Fast)</td>
</tr>
</tbody>
</table>
- Decoding error present.
- No decoding error.
- Only up (increasing) or down (decreasing) count is possible.
- It is also called as Ripple Counter. Ex - King Johnson Counter.
- Only JK or T Flip-Flop is used.
- Asynchronous Counter.

* Modulus of a Counter:

Mod of a counter represents number of state counted by counter.

\[
\text{mod}_a \quad \text{mod}_b \quad \text{mod}_z
\]

over all \( \text{mod} = \text{any} \) \( z \)

If the counters having mod \( a \), mod \( b \), mod \( z \) are cascaded, then overall mod is any \( z \).

Thus, a mod 78 counter can be implemented by:

(a) 6 number of mod 6 counter
(b) 13 number of mod 6 counter
(c) A mod 18 be a mod 6 counter [x]
(d) 13 mod of mod 18 counter.
\[
\begin{align*}
0 & \equiv \text{mod } 4 \quad \Rightarrow 2 \text{ no. of flip-flops} \\
\text{mod } 8 & \equiv 3 \quad \Rightarrow \text{No. of flip-flops} \\
\text{mod } 16 & \equiv 4 \quad \Rightarrow \text{No. of flip-flops} \\
N &= \phi \cdot n \quad \Rightarrow \text{no. of flip-flops} \\
\log N &= \log_2 n \\
\log_2 N &= n \log_2 2 \\
\log_2 N &= n \cdot 1 \\
\therefore \quad n &= \log_2 N \\
\text{or} \quad n \geq \log_2 N \\
\text{mod } 8 &= 3 \text{ flip-flop} \\
\text{mod } 7 &= 3.8 \text{ flip-flops} \\
2 &= 4 \text{ (too less)} \\
3 &= 3 \text{ (too less)}
\end{align*}
\]
1. These are used to count the number of clock pulses.
2. These are used to measure the width (time period).
3. These are used to measure the frequency of clock pulse.
4. These are used in biomedical.

* Asynchronous Counters:

In the asynchronous counter only one flip-flop will be applied by external clock, that flip-flop will be known as Least Significant Bit (LSB). The adjacent flip-flop will behave as Most Significant Bit (MSB).

\[
\begin{align*}
\text{clk} & \rightarrow Q \\
\text{down Counter} & \quad \text{clk} \rightarrow \overline{Q} \\
\text{Up Counter}
\end{align*}
\]

For e.g. Mod 4

\[
\begin{array}{c|cccc}
& 0 & 0 & 0 & 0 \\
\hline
0 & 0 & 1 & 0 & 1 \\
1 & 1 & 0 & 1 & 0 \\
\end{array}
\]

For the asynchronous counter design J-K or T flip-flop are used with applied input is equal to 1.

Mod-4 Up-Counter:
Mod-4 Up Counter by using J-K Flip-Flop:

Mod-4 = 2^2 \Rightarrow \text{No. of FF required} = 2.

\[ \begin{array}{c}
\text{CLK} \quad (x) \quad 0 \quad 0 \quad 0 \\
1 \quad 0 \quad 0 \quad 0 \quad 1 \\
0 \quad 0 \quad 0 \quad 1 \\
0 \quad 0 \quad 1 \quad 0 \\
0 \quad 1 \quad 0 \quad 0 \\
1 \quad 0 \quad 0 \quad 0 \\
0 \quad 1 \quad 0 \quad 1 \\
0 \quad 0 \quad 1 \quad 1 \\
0 \quad 0 \quad 0 \quad 1 \\
0 \quad 0 \quad 0 \quad 0 \\
\end{array} \]

\begin{align*}
\text{Initial state will be equal to final state if} \\
\text{no. of mod equal to no. of clock pulse.}
\end{align*}

\text{Design a Mod-4 up counter by using two edge triggered flip-flop.}
Design a Mod-8 up counter by using negative edge triggered J-K F.F.

\[ \text{Mod } 8 = 2^3 \]

Select the required F.F.

\[ \left( \begin{array}{c|cccc} 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 \end{array} \right) \]

Q. Mod-8 up counter by using +ve edge trigger using J-K F.F.
Design a Mod-8 down counter by using positive edge-triggered.

Design a Mod-8 down counter by using negative edge-triggered J-K FF.

down Counting.
A Mod-8 and a Mod-4 counters are cascaded. Identify the number of flip-flops required?

(a) 9  (b) 5  (c) 6  (d) 7

Total Mod = 8 x 4

So, 8 x 4 = 32

So, 8 x 4 = 32, thus no. of flip-flops required = 5.

Identify the Mod of counter for the given circuit diagram?

(a) Mod 32 Counter  (b) Mod 16 Counter

(c) Mod 8 down counter  (d) Mod 8 up counter

Reduction of State:

To reduce the no. of count sequence from the actual sequence by using same no. of flip-flops is called as reduction of state.

To reduce the no. of state, preset & clear are used.

Preset: It is used to display output 1.

Clear: It is used to display output 0.

Both will operate at high input.
Design a Mod-6 up counter by using negative edge triggered J-K flip-flops.

For Mod-6, no. of flip-flops = 3.

Design a Mod-5 up counter.

C1 = Q_3 Q_2
Qn 1: For the given circuit diagram, find the MOd of the counter?

Ans: Mod - 10 up counter.

<table>
<thead>
<tr>
<th>$Q_3$</th>
<th>$Q_2$</th>
<th>$Q_1$</th>
<th>$Q_0$</th>
</tr>
</thead>
<tbody>
<tr>
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</tbody>
</table>
Synchronous Counter:

Any signal count sequence is possible. Any flip-flop count be used for the design purpose. Operation is faster as compared to Asynchronous Counter.

\[ T_0 = 2T_{\text{clock}} \]

\[ f_0 = \frac{1}{T_{\text{clock}}} = \frac{f_{\text{clock}}}{2} \]

Output frequency of any flip-flop in the Asynchronous counter is given by:

\[ f_{\text{clock}} = \frac{f_{\text{input}}}{\text{MOD}} \]

For the given circuit diagram, find the output frequency of each flip-flop.
Question: For the given circuit diagram, find the output frequency. \( f_{out} = \frac{f_{clk}}{2} \), \( f_{out} = \frac{f_{clk}}{4} \), \( f_{out} = \frac{f_{clk}}{6} \).

Design a synchronous counter that counts by using D-flip-flops.

Steps for Counter Design:

1. Determine the count sequence.
2. Draw the state table.
3. Draw the excitation table.
4. Implement characteristic table for the given flip-flop.
5. Minimise the logic circuit by using K-map.
(i) No. of flip-flops = 2 (largest no. in $A = 8 \rightarrow 11$) so we need 2 flip-flops.

(ii) State Table

(iii) Excitation Table:

<table>
<thead>
<tr>
<th>$Q_n$</th>
<th>$Q_{n+1}$</th>
<th>$D_2$</th>
<th>$D_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
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<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Flip-Flops $\Rightarrow D_1$ and $D_2$

$D_2 = \overline{D_2}$

$D_1 = \overline{D_2} D_1 + D_2 \overline{D_2}$
For the given circuit diagram, identify the count sequence if initial state are (0, 0).

1. $D_2, D_1, Q_2, Q_1$
   - $D_2$ = 0
   - $D_1$ = 0
   - $Q_2$ = 0
   - $Q_1$ = 0
   - $Q_2 = 0 \oplus Q_2$
   - $Q_1 = Q_1 \oplus Q_1$

2. $D_2, D_1, Q_2, Q_1$
   - $D_2$ = 1
   - $D_1$ = 0
   - $Q_2$ = 1
   - $Q_1$ = 0

3. $D_2, D_1, Q_2, Q_1$
   - $D_2$ = 0
   - $D_1$ = 0
   - $Q_2$ = 0
   - $Q_1$ = 1

For the given circuit diagram, find the circuit sequence $Q_2, Q_1$. 

**Diagram:**

- $D_2, D_1, Q_2, Q_1$
- $J_2, Q_2$
- $K_2, Q_2$
- $J_1, Q_1$
- $K_1, Q_1$
- $C_{lk}$
(a) \[00, 01, 10, 00, 01, 10\]
(b) \[00, 01, 11, 00, 10, 11\]
(c) \[00, 10, 01, 00, 10, 01\]
(d) \[00, 01, 10, 11, 00, 01, 10, 11\]
(e) \[00, 11, 01\]

\[D = Q_2 \quad J_2 = Q_1 = k_2\]
\[K_1 = 1\]
\[J = \overline{Q_2}\]

\[\overline{Q_1} \quad k_2 \quad J_1 \quad k_1 \quad Q_2 \quad Q_1\]

\[K_2 = 1, \quad J_1 = 1\]
\[J_2 = \overline{Q_2}, \quad K_1 = Q_1\]
\[J_2, k_2, J_1, k_1, Q_2, Q_1\]

\[0\ 1\ 1\ 1\ 0\ 1\]
\[0\ 1\ 1\ 1\ 0\ 1\]
\[0\ 1\ 1\ 1\ 1\ 0\ 1\ 0\]

For the given circuit diagram, find the count sequence.
Find the count sequence for the given circuit.

\[ S_2 = Q_2, \quad D_1 = Q_1 \]

\[ D_2 = D_1 \quad \text{and} \quad \overline{D}_1 = \overline{Q}_1 \]

\[ S_2 = S_1 \quad \text{and} \quad Q_2 = Q_1 \]

\[ \overline{S}_1 = \overline{Q}_1 \quad \text{and} \quad \overline{R}_1 = \overline{Q}_1 \]

\[ S_2 = \overline{Q}_2 \]

\[ R_2 = R_2 \]

\[ R_1 = \overline{Q}_1 \]
<table>
<thead>
<tr>
<th>$s_2 R_2$</th>
<th>$s_1 R_1$</th>
<th>$\theta_2$</th>
<th>$\theta_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>

Output sequences: $00, 11, 00, 11, \text{etc.}$
**Network Theory**

\[ V = IR \quad \text{Voltage Drop from +ve to -ve voltage} \]

\[ V = -IR \quad \text{Voltage Rise if the voltage is increasing} \]

\[ V_L = L \frac{dI}{dt} \]

\[ V_L = -L \frac{dI}{dt} \]

\[ I = C \frac{dV_C}{dt} \]

\[ I = -C \frac{dV_C}{dt} \]

\[ V = V_a - V_b \]
\[ V_a - V_b = 8V \]

\[ V = V_a - V_b \]

\[ 3V = V_a - V_b \]

\[ 3 - 0 \text{ } \text{ } \text{ground} \]

\[ 0 = (-3) \]

\[ 5 - 2 \]

\[ 2 = (-1) \]

So infinite no. are possible.

It is not possible to calculate potential at any point whether it is possible to calculate potential difference between two points.

\[ V = IR \]

\[ I = \frac{V}{R} \]

\[ \frac{V_a - V_b}{R} \]

always used.

not used.

JNV-9008

Q. For the given network find current I
\[ P = \frac{V^2}{R} \quad \text{or} \quad P = VI \]

\[ I = \frac{V_a - V_b}{R} = \frac{1}{1\Omega} \]

\[ I = 1 \text{ Amp} \]

**Answer**

\[ P = VI \]

\[ P = -VI \]

**KVL**

Algebraic sum of all voltages in a closed loop is always equal to zero.

\[ -E_1 + IR_1 - E_2 + IR_2 = 0 \]

**Question**

For the given circuit diagram write the loop equation.
loop I : $-E_1 + I_1 R_1 + I_1 R_2 + (I_1 - I_2) R_3 + E_2 = 0$

loop II : $I_2 R_4 + I_2 R_5 + E_3 - E_2 - (I_1 - I_2) R_3 = 0$

or

$I_2 R_4 + I_2 R_5 + E_3 - E_2 + (I_2 - I_1) R_3 = 0$

(sign of $R_3$ (+ve) are considered)

Write the loop equation for the given circuit diagram.
Loop I:
\[ -3 + I_1 + I_1 (I_1 - I_3)^2 + (I_1 - I_2)^3 + 2 = 0 \]

\[ \Rightarrow \]

Loop II:
\[ I_2^2 + 5 - 2 + (I_2 - I_1)^2 + (I_2 - I_3)^4 = 0 \]

\[ \Rightarrow \]

Loop III:
\[ I_3 = 2 \text{ Amp} \]
Qms for the given circuit diagram find the currents $I_1, I_2, I_3$.

Loop I:

$$(I_1 - I_3) + (I_1 - I_2) - 3 = 0$$

$3I_1 - 2I_2 - I_3 = 3$  ...(I)

Loop II:

$$I_2 - (I_2 - I_1) + (I_2 - I_3) + 2 = 0$$

$2I_1 = 5I_2 + I_3 = 2$  ...(II)

Loop III:

$$5 + 3(I_3 - 2 + (I_3 - I_2) + (I_3 - I_1)) = 0$$

$-(I_1 - I_2) + 4I_3 = 2 - 5 = -3$

$I_1 + I_2 - 4I_3 = 3$  ...(III)
Op-Amp

Operational Amplifiers

Open Loop Op-Amp.
(Comparator)

Close Loop Op-Amp.

Positive feedback
(Amplifier)

Negative feedback

(U-235)

Nuclear Reactor

Nuclear Energy + HEAT

In the open loop connection there is no connection between output and input.

If there is a connection between output and input it is called as feedback. If the amount of input reduced from the actual amount is...
called Negative feedback if the amount of input is increased from the actual amount is called Positive feedback.

**Open Loop Op-Amp**

- **Non-Inverting Terminal**
- **Inverting Terminal**

Entering Input:

\[ V_1 + (-V_2) = V_o \]

\[ V_1 - V_2 = V_o \]

The basic operation of op-Amp to amplify the difference of input.

**Characteristic Properties of Open Loop Op-Amp**

1. **Open Loop Gain**

\[ A = \frac{V_o}{V_{in}} \]

\[ V_o = A \cdot V_{in} \]

\[ V_o = A(V_1 - V_2) \]
So ideal value of gain is must be infinity.

Case I :

\[ V_0 = A (V_1 - V_2) \]

\[ V_0 = \infty (V_1 - V_2) \]

say \[ V_1 = 5 \] \[ V_2 = 3 \] \[ \therefore V_1 > V_2 \]

So \[ V_0 = +\infty \]

\[ = +V_{sat} \]

Case II :

\[ V_0 = A (V_1 - V_2) \]

\[ V_0 = \infty (V_1 - V_2) \]

say \[ V_1 = 3 \] \[ V_2 = 5 \] \[ \therefore V_2 > V_1 \]

\[ V_0 = \infty (-V_0) \]

\[ \therefore \]

\[ V_0 = -\infty = -V_{sat} \]

* Transfer characteristic of Open loop Op-Amp.*
For the given op-amp network, draw the output waveform.

\[ V_i = \sin t \]

\[ V_{sat}^+ = +15V \]

\[ V_{sat}^- = -15V \]

For the given circuit diagram, draw the output waveform.

\[ V_i \]

\[ V_o \]

\[ V_{sat}^+ = +15V \]

\[ V_{sat}^- = -15V \]
**Question:** For the given circuit diagram, draw the output waveform.

**Solution:**

- $V_{sat} = +15V$
- $V_{sat} = -15V$
- $V_1 - V_2 = \ldots$
- $V_2 = -1$
The output of open loop op. Amp. will be a rectangular wave.

Thus, find the output waveform.

\[ \text{Sin} \]
\[ +15 \]
\[ \text{Out} \]
\[ -15 \]
\[ V_0 \]

\* Basic: \*

\[ V = IR \]

\[ I = I_{\text{max}} \]
[\[ I = 0 \]
[\[ V = V_{\text{max}} \]
[\[ V = I \times 0 = 0 \]
[\[ V = 0 \]
Note: For a D.C. source inductor will be replaced by a wire and capacitor is replaced by broken wire.

* Close Loop @ p - Amp. of Negative feedback?

To solve negative feedback connection assume inverting and non-inverting terminals are connected (virtual short).

**Inverting Amplifier:**

\[ V_{in} + \frac{R_f}{R_1} V_0 = 0 \]

\[ I_1 + I_2 = 0 \] \hspace{1cm} \{ \text{by KCL} \}

\[ \frac{V_{in}}{R_1} + \frac{V_0}{R_f} = 0 \]

\[ \Rightarrow \frac{V_{in}}{R_1} = -\frac{V_0}{R_f} \]

\[ \Rightarrow \frac{V_0}{R_f} = -\frac{V_{in}}{R_1} \]

\[ \Rightarrow \frac{V_0}{V_{in}} = -\frac{R_f}{R_1} \] \hspace{1cm} \text{gain of Inverting Amplifier.}

**Non-Inverting Amplifier:**

\[ V_{in} + \frac{R_f}{R_1} V_0 = 0 \]

\[ I_1 + I_2 = 0 \]

\[ \frac{V_{in}}{R_1} + \frac{V_0 - V_{in}}{R_f} = 0 \]

\[ \frac{V_0 - V_{in}}{R_f} = \frac{V_{in}}{R_1} \]
\[
\frac{V_o}{V_{in}} = R_f \left( \frac{1}{R_1} + \frac{1}{R_f} \right)
\]

\[
\frac{V_o}{V_{in}} = \left( 1 + \frac{R_f}{R_1} \right) = \text{Gain of Non-Inverting Amplifier.}
\]

For the given Op-Amp network, find the current \( I_o \);

\[
\frac{V_o}{V_{in}} = -\frac{R_f}{R_1} = -\frac{10k}{2k} = -5 \text{ K}
\]

\[
V_o = V_{in} \times -5 = 2 \times -5 = -10 \text{ V}
\]

\[
\frac{V_o}{V_{in}} = \left( 1 + \frac{R_f}{R_1} \right) = \left( 1 + \frac{10k}{2k} \right) = 11
\]

\[
V_o = 8 \times 11 = 88 \text{ V}
\]

\[
V_o = 88 \text{ V}
\]

\[
I_o = \frac{V_o}{R} \Rightarrow I_o = \frac{88 \text{ V}}{5k} = \frac{9.8}{5k} = 1.96 \text{ mA}
\]
Given the circuit diagram, find the output voltage $V_o$.

\[ V_{o1} = 1 + \frac{R_f}{R_1} = 1 + \frac{5R}{R} = 6 \]

\[ V_{o1} = 6V_{in} \]

\[ \frac{V_{o2}}{V_{in}} = -2 \]

\[ \Rightarrow \quad V_{o2} = -2V_{in} \]

\[ V_o = V_{o1} - V_{o2} = 6V_{in} - (-2V_{in}) = 8V_{in} \]

\[ \frac{V_o}{V_{in}} = 8 \]
\[ \frac{V_{o1}}{V_{in}} = -\frac{R_2}{R_1} = -\frac{3K}{1K} \]

\[ \frac{V_{o1}}{V_{in}} = -3 \]

\[ V_{o1} = -3 \times V_{in} = -3 \times 2 \]

\[ V_{o1} = -6 \]

\[ V_o = V_{o1} - 0 = -6 - 0 = -6 \]

\[ V_o = -6 \text{ Ans} \]

**Question:** For the given OP-Amp network, determine the output voltage. An answer is 1 V.

\[ V_{o1} \]

\[ V_o \]

\[ V_{in} \]

\[ V_{out} \]

\[ R_1 \]

\[ R_2 \]

\[ C \]

\[ 1V \text{ D.C.} \]
Q1 For the given circuit diagram, find the output voltage.

Since it is open loop, so the OP = saturation.

Q2 Find the output voltage for given circuit.

S1 \( V_{\text{in}} = 3\, \text{Vdc} \)

\[ V_{\text{out}} = \frac{3}{10} \, \text{Vdc} \]
\[
\frac{V_o}{V_{in}} = - \frac{R_4}{R_1} = -100K
\]

\[
\frac{V_o}{V_{in}} = -10 \implies V_o = -10 \times V_{in} = -10 \times 8 = -80V \text{ Ans}
\]

For the given network calculate the voltage gain.

\[
I_2 = I_3 + I_4
\]

\[
\frac{V_o - V_4}{R} = \frac{V_{a_1} - 0}{R} + \frac{V_{a_1} - 0}{R}
\]

\[
V_o = 8V_{a_1}
\]

\[
V_{a_1} = \frac{V_o}{8}
\]

\[
I_1 + I_4 = 0
\]

\[
\frac{V_{in} - 0}{R} + \frac{V_{a_1} - 0}{R} = 0
\]

\[
V_{in} = -V_{a_1}
\]

\[
V_{in} = -\frac{V_o}{8}
\]

\[
\frac{V_o}{V_{in}} = -8 \text{ Ans}
\]
For the given network, find the voltage gain.

\[ V_o = 8V_y - V_y = 9V_y - V_y = 8V_y \]

\[ V_0 = 8V_y \]

\[ V_y = \frac{V_0}{9} \]

\[ I_2 = I_3 + I_4 \]

\[ \frac{V_0 - V_a}{R} = \frac{V_a - V_y}{R} + \frac{V_y}{R} \]

\[ V_0 = 8V_a - V_y \]  \( \text{Equation 1} \)

\[ \text{Now } I_5 = I_3 + I_6 \]

\[ \frac{V_a - V_y}{R} = \frac{V_y - 0}{R} + \frac{V_y - 0}{R} \]

\[ V_a = 3V_y \]  \( \text{Equation 11} \)

From Equation 11 and Equation 1:

\[ V_5 = 3 \times 3V_y - V_y = 8V_y \]

\[ V_0 = 8V_y \]

\[ V_y = \frac{V_0}{9} \]
\[ I_1 + I_6 = 0 \]

\[ \frac{V_{in} - 0}{R} + \frac{V_Y}{R} = 0 \]

\[ V_{in} = -V_Y \]

\[ V_{in} = -\frac{V_0}{8} \]

\[ \frac{V_0}{V_{in}} = -8 \]

**Question:** For the given circuit diagram, determine o/p voltage.

**Solution:**

![Circuit Diagram]

- The circuit is called **voltage follower** (o/p voltage always follow i/p voltage).

\[ \frac{V_0}{V_{in}} = 1 \]

- It is also called as **Unity gain Amp**.
- Voltage follower is used to convert high impedance source to low impedance source.
Properties of Op-Amp.

* Input Current:

The input resistance of the op-amp will be infinity (represented by input circuit) hence input current will be zero. Voltage will be maximum.

\[
\begin{align*}
\frac{v_1}{v_2} & \quad \text{Input Current} \\
\text{Input voltage} & \quad \text{Input Current}
\end{align*}
\]

\(\text{Input resistance will be } \infty\).

* Output Resistance:

The output resistance of op-amp will be ideally zero.

\[
\begin{align*}
v_1 & \quad \text{Output resistance} \\
v_2 & \quad \text{Output Voltage}
\end{align*}
\]

\(\text{Output resistance is } 0\).

For the given circuit diagram find output voltage.

\[
\begin{align*}
R & \\
-\frac{v_2}{v_1} & \quad \text{Input voltage}
\end{align*}
\]

\(I = 0\)

\(\frac{v_2}{v_1} = 0\)

\[
\begin{align*}
\frac{v_0}{v_{in}} & = 0 \\
R & \\
\text{voltage follower}
\end{align*}
\]
For the given Op-Amp determine the Op voltage.

\[ V_0 = -V + IR_1 + IR_2 = 0 \]

\[ I = \frac{V}{R_1 + R_2} \]

\[ V_1 = IR_1 \]

\[ V_1 = \frac{V R_1}{R_1 + R_2} \] (memorize)

\[ V_2 = IR_2 \]

\[ V_2 = \frac{V R_2}{R_1 + R_2} \] (memorize)

So \[ V_m = \frac{5 \times 9.0}{8} = \frac{10}{3} \text{ volt} \]

\[ \Rightarrow I_1 + I_2 = 0 \]
\[
\frac{3-V_{in}}{20k} + \frac{V_{0}-V_{in}}{10k} = 0
\]

\[
8-V_{in} + \frac{V_{0}-V_{in}}{2} = 0
\]

\[
8-V_{in} + \frac{V_{0}-V_{in}}{2} = 0
\]

\[
\frac{V_{0}}{2} = \frac{3V_{in}}{2} - 3
\]

\[
\frac{V_{0}}{2} = \frac{3 \times 10^{-5}}{2 \times 8} - 3
\]

\[
\frac{V_{0}}{2} = 5 - 3 = 2
\]

\[
V_{0} = 2 \times 2 = 4
\]

\[
V_{0} = 9
\]

**Trick:**

When \( \frac{R_{f}}{R_{1}} = \frac{R_{3}}{R_{2}} \) then \( V_{0} = (V_{in}-V_{-}) \left( \frac{R_{f}}{R_{1}} \right) \) (Memorise)

\[
V_{0} = (5-3) \left( \frac{2}{2} \right)
\]

\[
V_{0} = 2 \times 2
\]

\[
V_{0} = 4 \text{ V}
\]
Find the output voltage.

\[ \frac{R_f}{R_1} = \frac{R_3}{R_2} = 2 \]

\[ V_0 = (7 - 3) \times 2 = 4 \times 2 \]

\[ V_0 = 8 \]

For the given circuit diagram determine output voltage.

\[ V_u = \frac{90 \times 7}{20 + 50} = \frac{630}{70} = 9 V \]

by KCL:

\[ I_1 + I_2 = 0 \]

\[ \frac{V_u - 3}{20} + \frac{V_0 - V_u}{60} = 0 \]

\[ -V_0 = \frac{60 \times 5}{12} - \frac{19 \times 16}{3} \]

\[ V_0 = -7 \frac{9}{3} - \frac{15 - 19}{3} \]

\[ V_0 = 1.83 V \]
(1) \[ -110V + I_1 \cdot 8 \Omega + (I_1 - I_3) \cdot 1 \Omega + (I_3 - I_2) \cdot 5 \Omega = 0 \]

(2) \[ 2I_1 + I_3 = I_3 + 5I_1 - 5I_3 = 110 \]

(3) \[ 8I_1 - 6I_3 = 110 \]

(4) \[ -115 + I_3 \cdot 6 \Omega + (I_3 - I_1) \cdot 1 \Omega = 0 \]

(5) \[ 7I_3 - I_1 = 155 \]

(6) \[ I_1 \cdot 5 \Omega + (I_2 - I_1) \cdot 5 \Omega = 0 \]

(7) \[ 10I_2 - 5 - I_1 = 0 \]
For the given circuit diagram calculate voltage gain.

\[ \frac{v_o}{v_{in}} = -\frac{R_4}{R_1} \]

For the given circuit diagram calculate \( v_o \).

(a) \( \sqrt{2} \sin (t + 90^\circ) \)
(b) \( \sqrt{2} \sin (t + 90^\circ) \)
(c) \( \frac{1}{\sqrt{2}} \sin (t - 90^\circ) \)
(d) \( \frac{1}{\sqrt{2}} \sin (t + 90^\circ) \)


\[ V_{in} = \sin(\omega t) = \sin t \]

\[ w = \frac{1}{\sqrt{L}} \]

\[ C = \frac{1}{j\omega C} = \frac{1}{\omega x 1} \]

\[ C = \frac{1}{j} \]

\[ V_{an} = \frac{\sin t \times \frac{j}{j+1}}{1+\frac{j}{j}} = \frac{\sin t}{1+j} \]

\[ V_{an} = \frac{\sin t \times \frac{j}{j+1}}{j+1} = \frac{\sin t}{1+j} \]

\[ V_{an} = \frac{\sin t \times \frac{j}{j+1}}{j+1} = \frac{\sin t}{1+j} \]

by KCL, \[ I_1 + I_2 = 0 \]

\[ 0 = \frac{V_{an}}{10K} + \frac{V_b-V_a}{10K} = 0 \]

\[ V_b - 2V_a = 0 \]

\[ V_0 = 2V_a \]

\[ V_0 = \frac{2 \sin t}{1+j} \]

\[ a+i b = \sqrt{a^2 + b^2} = \text{mag} \]

\[ \text{Phase} \ L = \tan^{-1}\left(\frac{b}{a}\right) \]

\[ |1+j| = \sqrt{1^2+1^2} = \sqrt{2} \]

\[ \text{Phase Angle} = -\tan^{-1}\left(\frac{1}{1}\right) \]

\[ \frac{a+j b}{d} = \frac{1}{d^2 + b^2} \]

\[ \text{Phase}\ L = -\tan^{-1}\left(\frac{b}{a}\right) \]

So, from (1)

\[ V_0 = \frac{2 \sin t}{1+j} \]

\[ 45^0 \]

\[ \frac{2 \sin t - 195^0}{\sqrt{2}} \]
For the given circuit diagram find the output maximum phase difference b/w o/p and i/p.

\[
V_o = \sqrt{2} \sin (\theta - 15^\circ)
\]

\[
V_o = \sqrt{2} \sin (\theta - 15^\circ)
\]

\[
\sin (\theta + \phi) = \sin (\theta - \phi)
\]

By KCL:

\[
I_1 + I_2 = 0
\]

\[
\frac{V_i - V_{o1}}{R} + \frac{V_o - V_{o2}}{R} = 0
\]

\[
V_o = 2V_{a} - V_i
\]

\[
V_o = \frac{2V_i - V_i}{1 + j\omega RC}
\]

\[
V_o = V_i \left( \frac{2}{1 + j\omega RC} - 1 \right)
\]
\[ V_o = V_i \left( \frac{2 - (1 + jwRC)}{1 + jwRC} \right) \]

\[ = V_i \left( \frac{2 - 1 - jwRC}{1 + jwRC} \right) \]

\[ V_u = V_i \left( \frac{1 - jwRC}{1 + jwRC} \right) \]

\[ \frac{V_o}{V_i} = \left[ \frac{1 - jwRC}{1 + jwRC} \right] \]

Phase Difference:

\[ \tan^{-1} \left( \frac{-wRC}{1} \right) - \tan^{-1} (wRC) \]

\[ = -\tan^{-1} (wRC) - \tan^{-1} (wRC) \]

\[ = -2 \tan^{-1} (wRC) \]

\[ \therefore \text{Maximum Phase Difference} = -2 \tan^{-1} (\infty) \]

becaue \( \tan \) \( \frac{\pi}{2} \) is maximum at 90°.

\[ = -2 \times 90° \]

\[ = -180° \]

\[ = +180° \text{ Arg} \]

\[ \begin{array}{c}
+90° -270° \\
+180° \end{array} \]

\[ +270° -90° \]
Note: The Voltage Short concept is useful when gain is not infinity.

For the given circuit diagram calculate the voltage gain.

**Solution**

\[
\frac{V_0}{V_{in}} = -\frac{R_2}{R_1} = \frac{1}{j\omega C} = \frac{-1}{j\omega RC}
\]

\[
\left| \frac{V_0}{V_{in}} \right| = \sqrt{1 + (j\omega C)^2} = \sqrt{\omega^2 C^2 R^2}
\]

\[
\left| \frac{V_0}{V_{in}} \right| = \omega CR
\]

Note: A network which produces high gain in low freq. gain range is called as Low Pass Filter.

High Frequency (High gain)

Low Frequency (High gain)

It is unstable filter because its gain reaches infinity at \(w = 0\).
Filter

* Practical Low Pass Filter :*

\[
\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}
\]

\[
R_{11\, \omega} = \frac{R_f \times \frac{1}{j\omega C_f}}{R_f + \frac{1}{j\omega C_f}} = \frac{R_f}{R_f + j\omega C_f}
\]

\[
R_{11,\omega} = \frac{R_f}{1 + R_f j\omega C_f}
\]

So \[
\frac{V_o}{V_{in}} = -\frac{R_f}{1 + R_f j\omega C_f} = \frac{R_f}{R_f + j\omega C_f}
\]

\[
\left|\frac{V_o}{V_{in}}\right| = \frac{R_f}{R_1 \sqrt{1 + \omega^2 C_f^2 R_f^2}}
\]

Low Freq. Region
Question:

For the given circuit diagram, calculate the magnitude of voltage gain and phase difference $\theta$ between output and input.

![Circuit Diagram]

(a) $10, \pi/2$
(b) $10, -\pi$
(c) $-10, \pi/2$
(d) $5\sqrt{2}, -\pi/2$

Solution:

**Voltage Gain**

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1(1+j\omega R_f C_f)}$$

$$\frac{V_o}{V_{in}} = \frac{-R_f}{R_1(1+j2\pi f R_f C_f)}$$

$$\left| \frac{V_o}{V_{in}} \right| = \frac{R_f}{R_1 \sqrt{1+ (8.14)^2 (10)^2 (10)^2 (0.0001 \times 10^4)}}$$

$$\approx \frac{R_f}{R_1 \sqrt{1+ 4(8.14)^2 (10)^2 (10)^2 (0.0001 \times 10^4)}}$$

$$\approx \frac{10 \sqrt{1+ (8.14)^2 (10)^2 (10)^2 (0.0001 \times 10^4)}}{10}$$

Very small $\omega$

$$\left| \frac{V_o}{V_{in}} \right| = 10$$

Answer:

$$\left| \frac{V_o}{V_{in}} \right| = 10$$
Phase Angle:

\[
\frac{V_o}{V_{in}} = \frac{R_1}{R_1 \left(1 + j\omega R_1 C_f\right)} = \frac{-10k}{1K \left[1 + j \cdot 2\pi \cdot 1 \times 10^6 \cdot 1 \times 10^{-6}\right]} = \frac{-10}{1 + j \cdot 6.25 \times 10^5} = \frac{-10}{1 + j \cdot 0.000628}
\]

\[
\angle \frac{V_o}{V_{in}} = 180^\circ - \tan^{-1}\left(\frac{0.000628}{1}\right) = 180^\circ - \tan^{-1}(0) = 180^\circ - 0
\]

\[
\text{Phase diff.} = 180^\circ
\]

Question: Find the voltage gain of the given circuit.
\[ \frac{V_o}{V_{in}} = -\frac{R_f}{R_i} \]

\[ = -\frac{R}{1+j\omega C} \]

\[ = -j\omega CR \]

\[ \left| \frac{V_o}{V_{in}} \right| = \omega RC \]

Since gain reaches to infinity at \( \omega \to \infty \), so it becomes unstable (Impractical).

**Practical High Pass Filter:**

\[ V_{in} \quad R \quad C_1 = \frac{1}{j\omega C_1} \quad R_f \quad R \quad V_o \]

\[ \frac{V_o}{V_{in}} = -\frac{R_f}{R_i} \]

\[ R_{series} = R + \frac{1}{j\omega C} \]

\[ = \frac{j\omega R_i C_1}{j\omega C_1} \]

\[ = \frac{1+j\omega R_i C_1}{j\omega C_1} \]
\[
\frac{V_o}{V_{in}} = \frac{R_f \cdot w \cdot c_1}{\sqrt{1 + w^2 R_f^2 c_1^2}} \cdot \frac{1}{\sqrt{1 + \frac{w^2 R_f^2 c_1^2}{w^2 R_f^2 c_1^2}}} \\
= \frac{1}{\sqrt{(w R_f c_1)^2 + \frac{w^2 R_f^2 c_1^2}{R_f^2 c_1^2}}} \\
= \frac{1}{\sqrt{(w R_f c_1)^2 + \frac{R_f^2}{R_f^2 c_1^2}}} \\
= \frac{\frac{R_f}{R_f}}{\sqrt{1 + \left(\frac{w R_f c_1}{R_f}\right)^2}} \\
= \frac{V_o}{V_{in}} = \frac{R_f}{R_f} \sqrt{1 + \frac{1}{(w R_f c_1)^2}}
\]
Practical High Pass Filter

\[
\frac{V_o}{V_{in}} = \frac{R_1}{R_1 \sqrt{1 + (\omega R C_f)^2}}
\]

Unstable:

\[
C \rightarrow R \rightarrow H.P.F.
\]

\[
R \rightarrow C \rightarrow L.P.F.
\]

Short Trick: Practical OR Stable Filter:
A B.P.F. is represented by its mid-frequency $w_0$ it is implemented by using H.P.F. and L.P.F. If the cut-off frequency of L.P.F. is $w_{LP}$ and H.P.F. is $w_{HP}$ then which of the following will satisfy for band pass filter.

(a) $w_0 > w_{LP} + w_{0 > w_{HP} \}$ (c) $w_0 < w_{LP} + w_{0 > w_{HP} \}$

(b) $w_0 > w_{LP} + w_{0 < w_{HP} \}$ (d) $w_0 < w_{LP} + w_{0 < w_{HP} \}$
Draw for the given circuit diagram identify the type of filter.

Band Pass Filter.

Draw for the given circuit diagram identify the filter.
\[
V_{o} = \frac{V_{in} \cdot \frac{1}{j \omega C}}{R + \frac{1}{j \omega C}} = \frac{V_{in}}{1 + R j \omega C}
\]

\[
V_{o} = \frac{V_{in}}{1 + R j \omega C}
\]

By KCL:

\[
I_1 + I_2 = 0
\]

\[
\frac{D - V_{o1}}{R_1} + \frac{V_0 - V_{in}}{R_2} = 0
\]

\[
V_0 = \frac{V_{in} + V_{o1}}{R_1}
\]

\[
V_0 = \frac{V_{in}}{R_1} \left( \frac{1}{R_1 + R_2} \right)
\]

\[
\frac{V_0}{R_2} = \frac{V_{in}}{1 + R j \omega C \left( \frac{1}{R_1 + R_2} \right)}
\]

\[
\frac{V_0}{V_{in}} = \frac{R_2}{1 + j \omega R C \left( 1 + \frac{R_2}{R_1} \right)}
\]
\[ \left| \frac{V_o}{V_{in}} \right| = \frac{(1+ \frac{R^2}{R_1^2})}{\sqrt{1 + \omega^2 R^2 C^2}} \]

when \( \omega \) increasing, \( \frac{V_o}{V_{in}} \) decreasing

So it is how Parks Filter.

\[ \frac{R_b}{R_1} \]

for the given circuit diagram identify the filter.

\[ V_{oa} = \frac{V_{in} R_2}{R + \frac{1}{j \omega C}} = \frac{V_{in} (j \omega R C)}{1 + j \omega R C} \]
\[ \frac{-V_{m}}{R_{1}} = \frac{V_{o}}{R_{2}} - \frac{V_{o}}{R_{2}} \]

\[ \frac{V_{o}}{R_{2}} = V_{m} \left( \frac{1}{R_{2}} - \frac{1}{R_{1}} \right) \]

\[ V_{o} = \frac{V_{in} \cdot R}{R + \frac{1}{j\omega C}} \left( \frac{1}{R_{2}} - \frac{1}{R_{1}} \right) \]

\[ \frac{V_{o}}{V_{in}} = \frac{R_{2} \cdot R}{(R + \frac{1}{j\omega C}) \cdot R_{2}} \left( \frac{1 - \frac{R_{2}}{R_{1}}}{1 - \frac{R_{2}}{R_{1}}} \right) \]

\[ \frac{V_{o}}{V_{in}} = \left( 1 - \frac{R_{2}}{R_{1}} \right) \left( 1 - \frac{1}{j\omega C} \right) + \sqrt{1^2 + \frac{1}{j\omega C} R_{2}^2} \]

\[ \frac{V_{o}}{V_{in}} = \frac{1 + \frac{R_{2}}{R_{1}}}{1 + \left( \frac{1}{j\omega C} \right)^2} + 1, \quad \frac{V_{o}}{V_{in}} = \sqrt{1 + \left( \frac{1}{j\omega C} \right)^2} + 1, \quad F \]
The frequency at which gain reduced by a factor of $\frac{1}{2}$ that frequency is called as "cut-off frequency" and is given by:

$$\omega_c = \frac{1}{R_f C_f}$$

This factor $\frac{1}{2}$ also represents 3 dB decrease which is given

$$\frac{10}{\pi^2} \approx 20 \log \left( \frac{10}{\pi^2} \right) \text{ dB}$$

$$= 20 \left[ \log 10 - \log \sqrt{2} \right]$$

$$= 20 \left[ 1 - 0.15 \right]$$

$$= 17 \text{ dB}.$$
The cut-off freq. defines the freq. after which gain decreases (L.P.F.) and gain increases (H.P.F.).

For the given circuit diagram identify the type of filter and calculate the cut-off frequency (Hz).

\[ V_x = \frac{V_{in} \times j\omega C}{R + \frac{1}{j\omega C}} = \frac{V_{in} \times j\omega C}{Rj\omega C + 1} \]

\[ V_x = \frac{V_{in}}{1 - j\omega RC} \]

By KCL:

\[ I_1 + I_2 = 0 \]

\[ 0 - \frac{V_a}{1K} + \frac{V_o - V_{in}}{10K} = 0 \]

\[ \frac{V_o}{10} = V_{in} + \frac{V_a}{10} \]

\[ \frac{V_o}{10} = V_{in} \left( \frac{11}{10} \right) \]

\[ V_o = \frac{11V_{in}}{1 + j\omega RC} \]
\[ \frac{U_o}{V_{in}} = \frac{11}{1 + j\omega RC} \]

\[ \left| \frac{U_o}{V_{in}} \right| = \frac{11}{\sqrt{1 + \omega^2 R^2 C^2}} \]

Hence filter is L.P.F.

Cut off frequency \( \omega_c = \frac{1}{RC} \)

\[ \omega_c = \frac{1}{1 \times \frac{1}{2 \pi} \mu F} \]

\[ \omega_c = \frac{2 \pi \times 1 \mu F}{2 \pi \times 1 \times 1 \mu F} \]

\[ \omega_c = 2 \pi \times 1 \mu F \]

\[ \left\{ \begin{array}{l} \omega_c = \frac{10^6}{10^8} \\ 1 \text{Hz} = \frac{10^9}{10^8} \end{array} \right. \]

\[ \frac{\nu_c}{f_c} = 1 \text{ kHz} \]

For the given circuit diagram taken

Calculate the D.C. gain:

\[ \text{D.C. gain for Non-Inverting Amp.} = (1 + \frac{R_6}{R_1}) \]

\[ \text{D.C. gain} = (1 + \frac{10^3}{10^3}) \]

\[ \text{D.C. gain} = 11 \]
\[ V_o = \frac{V_{in} R_1 C}{1 + \frac{R_1}{R_2}} \]

\[ V_o = \frac{V_{in}}{1 + \frac{R_1}{R_2}} \]

By KCL:
\[ -\frac{V_o}{R_1} + \frac{V_{in}}{R_2} = 0 \]

\[ V_{in} = \frac{V_o}{R_2} \]

\[ I_2 = \frac{V_o}{R_2} \]

\[ I_1 = \frac{V_{in} R}{R_2} \]

\[ V_{in} R = \frac{V_o R}{R_2} \]

\[ V_{in} = \frac{V_o}{R_2} \]
\[
\frac{V_o}{V_{in}} = \frac{wRC}{\sqrt{1 + (wRC)^2}} \left( 1 + \frac{R_F}{R_i} \right)
\]

\[
\omega_c = \frac{1}{RC}
\]

for D.C. gain.

Capacitor change into breaked wire.
In break wire current is zero but voltage is maximum so resistance have zero voltage.
So the terminal have \(V_{in}\).

D.C. gain for non-inverting amplifier is \((-\frac{R_F}{R_i})\) and for inverting amplifier

For the given circuit diagram, identify the filter.

\[
\frac{V_o}{V_{in}} = -\frac{R_f}{R_1} = -\frac{R_S}{R_1} \quad (R_S = R_f + j\omega L)
\]

\[
\left| \frac{V_o}{V_{in}} \right| = \frac{\sqrt{R_f^2 + (\omega L f)^2}}{R_1}
\]

\[
= \frac{R_f}{R_1} \sqrt{1 + \left( \frac{\omega L f}{R_f} \right)^2} = \frac{R_f}{R_1} \sqrt{\left( \frac{R_f}{R_1} \right)^2 + \left( \frac{\omega L f}{R_f} \right)^2}
\]

\[
\omega = \frac{R_f}{L f}
\]

\[
\begin{align*}
\omega_c &= \frac{1}{2\pi} \frac{R_1}{R_f}
\end{align*}
\]
Gain for the given circuit diagram identify the type of filter.

\[
\frac{V_0}{V_{in}} = -\frac{R_f}{R_1} = -\frac{R_f}{R_{11,del}}
\]

\[
= -\frac{R_f}{\frac{R_1 - j\omega L_1}{R_f + j\omega L_1}} = -\frac{R_f (R_f + j\omega L_1)}{R_1 - j\omega L_1}
\]

\[
\left|\frac{V_0}{V_{in}}\right| = \frac{R_f}{R_1} \sqrt{\frac{R_1 + (\omega L_1)^2}{\omega L_1}} = \frac{R_f}{R_1} \sqrt{1 + \frac{R}{(\omega L_1)^2}}
\]

Since gain decreases so L.P.F.

Gain decreases.
Ans. for the given circuit diagram, calculate the output voltage. \( R = C \)

\[
\begin{align*}
V_{in} & \quad + \quad R_1 \quad \downarrow \\
\quad \downarrow & \quad C_1 \\
\quad + & \quad I_1 \quad \downarrow \\
\quad \downarrow & \quad C_2 \\
\quad + & \quad V_o \\
\quad \downarrow & \quad R \\
\quad \downarrow & \quad E
\end{align*}
\]

By KCL:

\[ I_1 + I_2 = 0 \]

\[
\frac{V_{in} - 0}{R_1} + C_1 \frac{dV}{dt} = 0
\]

\[
V_{in} + C_1 \frac{dV}{dt} = 0
\]

\[ (V = V_0 - 0) \]

\[ \text{means } V = V_0 \]

\[ \therefore \frac{V_{in}}{R_1} + C_1 \frac{dV_0}{dt} = 0 \]

\[
C_1 \frac{dV_0}{dt} = -\frac{V_{in}}{R_1}
\]

\[
\frac{dV_0}{dt} = -\frac{1}{R_1 C_1} V_{in} \quad \text{dt}
\]

\[
\int dV_0 = \int -\frac{1}{R_1 C_1} V_{in} \quad \text{dt}
\]
The behaviour of a low pass filter is similar to an integrator circuit.

\[ V_0 = -\frac{1}{RC} \int V_{in} \, dt \]

\[ C = R \]

\[ i \text{ H.P.F. ?} \]

**Solution:**

By KCL:

\[ I_1 + I_2 = 0 \]

\[ C \frac{dv}{dt} + \frac{V_0}{R} = 0 \]

\[ \frac{V_0}{R} = -C \frac{dv}{dt} \]

\[ V_0 = -CR \frac{dv}{dt} \]

\[ \therefore V_{in} = V - 0 \]

So, \[ V = V_{in} \]

\[ V_0 = -RC \frac{dV_{in}}{dt} \]

The behaviour of a high pass filter is a differentiator.
The diagram illustrates the relationship between functions and their derivatives or integrals. The notations and symbols are as follows:

- **U(x)**: Likely a function or variable.
- **Step function**: A function that increases or decreases suddenly.
- **Discrete delta function**: A function that is zero everywhere except at a single point.
- **Integrating**: The process of finding the area under a curve or summing infinitesimal quantities.
- **Differentiating**: The process of finding the rate at which a function changes with respect to its input.
- **Ramp function**: A linearly increasing function.

The text below the diagram explains the relationship:

- **Ramp** → **Step** → **Dirac Delta**
- **Ramp** ← **Step** ← **Dirac Delta**
The i/p, o/p waveform represented below.

(i) Adder  (ii) Subtractor  (iii) Integrator
(iv) Differentiator

2.2 For the given circuit diagram find the output current waveform.
Calculate output voltage.

\[ I_1 + I_2 + I_3 + I_4 = 0 \]

\[ \frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} + \frac{V_0}{R_f} = 0 \]

\[ \frac{V_0}{R_f} = -\left(\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R}\right) \]

\[ \frac{V_0}{R_f} = -\frac{1}{R} \left(V_1 + V_2 + V_3\right) \]
An inverting summing amplifier output $V_o = -0.1V_1 - 0.2V_2 - 0.4V_3$, if $R_f = 10k$

Calculate $R_1, R_2, R_3$. 

\[ V_o = \frac{-R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2 - \frac{R_f}{R_3} V_3 \]

\[ \frac{R_f}{R_1} = 0.1 \]

\[ R_1 = \frac{R_f}{0.1} = \frac{10}{0.1} = 100k \Omega \]

\[ R_1 = 100k \Omega \]

\[ \frac{R_f}{R_2} = 0.2 \]

\[ R_2 = \frac{10}{0.2} = 50 \Omega \]

\[ R_2 = 50k \Omega \]

\[ \frac{R_f}{R_3} = 0.4 \]

\[ R_3 = \frac{10}{0.4} = 25 \Omega \]

\[ R_3 = 25k \Omega \]
Run for the given circuit diagram calculate output voltage.

\[ I_1 + I_2 + I_3 = 0 \]
\[ \frac{V_1 - V_a}{R} + \frac{V_2 - V_a}{R} + \frac{V_3 - V_a}{R} = 0 \]

\[ V_a = \frac{V_1 + V_2 + V_3}{3} \]

By k.c.l.
\[ I_4 + I_5 = 0 \]
\[ \frac{0 - V_a}{R_1} + \frac{V_2 - V_a}{R_F} = 0 \]
\[ \frac{V_2}{R_F} = V_a \left( \frac{1}{R_1} + \frac{1}{R_F} \right) \]
\[ V_o = V_a \left( 1 + \frac{R_F}{R} \right) \left( \frac{V_1 + V_2 + V_3}{3} \right) \]

Averaging amp. is also non-inverting summing amp.
For the given circuit diagram calculate the current $I_3$.

\[ I_1 + I_2 = 0 \]

\[ \frac{0}{1k} + \frac{V_0 - 0}{2k} = 0 \]

\[ V_0 = -2 \]

\[ V_0 = -4 \]

\[ I_2 = -\frac{4-0}{2k} = -2mA \quad (\text{with direction of flow of current is opposite}) \]

\[ I_2 = \frac{0 - (-4)}{2k} = \frac{4}{2} = 2mA \]

\[ I_3 = 2mA. \]
\[ I + I_2 + I_3 = 0 \]

\[ I + 2 + 2 = 0 \]

\[ I = -4 \text{ mA} \]

**Question:** For the given circuit diagram, calculate the current through each and every branch.

\[ 5V \quad I_1 \quad + \quad I_2 \quad + \quad I_3 \quad = \quad 0 \]

\[ \frac{5 - 0}{V} + \frac{V_0 - 0}{S} + \frac{V_0 - 0}{2K + 8K} = 0 \]
Calculate currents from each branch.
For the given circuit diagram calculate the output voltage.

(i)

(ii)

2.2 For the given circuit diagram calculate the voltage gain and determine the type of filter.

\[ \frac{V_o}{V_{in}} = \frac{1}{(s+\omega_b)(s+\omega_c)} \]

2.3 For the given op-amp network find the current \( I \).
Q.2 Assume OP-AMP to be Ideal, what is the value of current $I$, through 5kΩ resistor?

\[ I_1 + I_2 = 0 \]
\[ I_2 = \frac{V_0 - 0}{2kΩ} \]
\[ V_0 = -2V \]
\[ I_2 = -1mA \]
\[ I_3 = \frac{V_0 - 0}{2kΩ} \]
\[ I_3 = -1mA \]
\[ I = I_2 + I_3 = 0 \]
\[ I + 1mA + 1mA = 0 \]
\[ I = -2mA \]
\[ V_0 = \frac{-R_2}{R_1} \]

\[ V_0 = -5 \times -1 \]

\[ V_0 = +5V \]

Question 12:
Calculate the value of \( c \) if \( w = 1000 \text{ rad/sec} \), \( R = 100 \text{ k}\Omega \), \( R_1 = 100 \text{ k}\Omega \), and phase shift between \( V_0 \) and \( V_i \) is 270°.

\[ c = \frac{1}{j\omega C} \]

\[ V_{in} = \frac{\gamma_{in}}{1 + j\omega CR} \]

\[ I_1 + I_2 = 0 \]

\[ \frac{V_{in} - V_{an}}{R_1} + \frac{V_0 - V_{an}}{R_1} = 0 \]

\[ \frac{V_{in}}{R_1} - \frac{V_0}{R_1} + \frac{2V_0}{R_1} \]

\[ V_0 = 2V_{an} - V_{in} \]

\[ V_0 = \frac{2V_{in}}{1 + j\omega CR} - V_{in} \]
\[ \frac{V_o}{V_{in}} = \frac{2}{1+j\omega RC} - 1 \]

\[ \frac{V_o}{V_{in}} = \frac{1-j\omega RC}{1+j\omega RC} \]

\[ = \frac{1+j(-\omega RC)}{1+j\omega RC} \]

\[ = \tan^{-1}(-\omega RC) - \tan^{-1}(\omega RC) \]

\[ = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC) \]

\[ = -2\tan^{-1}(\omega RC) \]

\[ -2\tan^{-1}(\omega RC) = -135^\circ \]

\[ \tan^{-1}(\omega RC) = -135^\circ \]

\[ \omega RC = \tan(-135^\circ) \]

\[ 1 \times 100 \times \frac{1}{10} \times \frac{1}{100} \times C = \tan(-135^\circ) \]

\[ C = \frac{\tan(-135^\circ)}{100 \times 10} \]

\[ C = \]
By Voltage divider Rule:
\[ \frac{-V_{in} + 0 - V_{a}}{1} = 0 \]

\[ 1 = 2V_{a} \]
\[ V_{a} = \frac{1}{2} = 0.5 \text{ V} \]
\[ V_{in} = 0.5 \text{ V} \]

\[ J_1 + J_2 = 0 \]
\[ \frac{10 - 0.5^+}{1k} + \frac{V_o - 0.5^-}{2k} = 0 \]
\[ \frac{V_o - 0.5^-}{2} = -0.5^- \]
\[ V_o = -0.5^- \text{ V} \]

\[ V_o = -0.5^- \text{ V} \]
\[ V_0 = (V_+ - V_-) \left( \frac{R_4}{R_1} \right) \]

- Amplification factor \( A \) same:
  \[ \frac{R_4}{R_1} = \frac{R_3}{R_2} \]
  \[ \frac{2.2}{10} = \frac{R}{15} \]
  \[ R = \frac{2.2 \times 15}{10} = 33 \Omega \]
  \[ R = 33 \, \text{k}\Omega \]

2.35 Which of the following pairs is/are correctly matched?

<table>
<thead>
<tr>
<th>Waveform</th>
<th>Circuitry and input signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Triangular wave</td>
<td>Integrating circuit and square wave</td>
</tr>
<tr>
<td>2. Impulsive wave</td>
<td></td>
</tr>
<tr>
<td>3. Saw tooth wave</td>
<td></td>
</tr>
</tbody>
</table>

(a) 2 and 3  (b) 1 and 2  (c) 1 alone  (d) 1 and 3

2.38 The output \( V_0 \) of the ideal op amp circuit shown in the figure is:

\[ \begin{array}{c}
V_0 \end{array} \]
\[
\frac{1}{1-V_{a_t}} + \frac{0}{V_{a_t}} = 0
\]

\[
\pm 2 V_{a_t} = -1
\]

\[
V_{a_t} = \frac{1}{2} = 0.5
\]

\[
V_a = 0.5 \text{V}
\]

By K.G.L

\[I_1 + I_2 = 0\]
So \[ f_c = 2 \text{kHz}, \quad A = 1.5 \]

\[ \omega_c = \frac{1}{R_c} \]

\[ \frac{\omega_c}{f_c} = \frac{1}{R_c} \]

\[ f_c = \frac{1}{\omega_c R_c} \]

\[ f_c = \frac{1}{2\pi R_2 C} \]

\[ R_2 = \frac{1}{2 \pi \times 2 \times 10^3 \times 0.097 \times 10^3} \]

\[ = \frac{10^6}{9 \times 10^3 \times 9.7 \times 10^3 \times 10^6} \]

\[ = \frac{10^6}{9 \times 8.14 \times 10^7} \]

\[ = \frac{10^6}{9 \times 8.14 \times 10^7} \]

\[ = 1.7 \text{k} \]

D.C. gain = \[ 1 + \frac{R_f}{R_1} \]

\[ 1.5 = 1 + \frac{R_f}{R_1} \]

\[ \frac{R_f}{R_1} = 0.5 \]
\[ R_1 = \frac{R_c}{\beta b} = 2R_f \]

\[ R_1 = 2 \times 15 \text{ k}\Omega \]

\[ R_1 = 30 \text{ k}\Omega \]

---

By K.C.L.

\[ I_1 + I_2 = 0 \]

\[ \frac{V_i - V_{o1}}{R} + \frac{V_o - V_{o1}}{R} = 0 \]

\[ V_0 = 2V_{o1} - V_i \]

\[ V_o = \frac{2V_{o1}R_2}{(R_1 + R_2)} - V_i \]

---

\[ V_o = -V_i + \frac{V_2}{2} \]
So arranging in given text:

\[ V_0 = -V_1 + \frac{V_2}{2} \left( \frac{R_2}{R_2 + R_1} \right) \]

\[ -V_1 + \frac{V_2}{2} = -V_1 + \frac{V_2}{2} \frac{2}{1 + \frac{R_1}{R_2}} \]

So \[ \frac{R_1}{R_2} = \frac{1}{2} \]

\[ \text{(b) Buffer Amp.}\]

\[ \text{(C) Adder} \]

\[ \text{Subtractor} \]

\[ \text{(D) Divider} \]

\[ I_1 + I_2 = 0 \]

\[ \frac{V_1 - 0}{R} + \frac{V_2 - 0}{R} \]

\[ V_0 = -V_1 \]

\[ I_3 + I_4 = 0 \]

\[ -\frac{V_1 + V_2}{R} + \frac{V_0 - V_2}{R} = 0 \]
\[ V_0 = V_1 + 2V_2 \]

So it's an adder.

By Kirchhoff's Voltage Law,

\[ V_0 = -\frac{R_4}{R_1} (V_a + V_b + V_c) \]

\[ = -\frac{R}{3R} (V_a + V_b + V_c) \]

\[ \Rightarrow \quad V_0 = -\frac{1}{3} (V_a + V_b + V_c) \]

\[ V_{o1} = \frac{1}{3} [V_a + V_b + V_c] \]
I_1 + I_2 + I_3 + I_4 = 0

\frac{V_a - V_{a_1}}{R} + \frac{V_b - V_{a_1}}{R} + \frac{V_c - V_{a_1}}{R} + \frac{O - V_{a_1}}{R} = 0

V_a - V_{a_1} + V_b - V_{a_1} + V_c - V_{a_1} = 0

q \cdot V_a = V_a + V_b + V_c

V_{a_1} = \frac{1}{q} \left[ V_a + V_b + V_c \right]

\frac{V_b - V_{a_1}}{R} + \frac{V_b - V_{a_1}}{3R} = 0

\frac{1}{3} \left[ V_a + V_b + V_c \right] - \frac{1}{q} \left[ V_a + V_b + V_c \right] + V_{a_1} = \frac{1}{q} \left[ V_a + V_b + V_c \right] = 0

\frac{V_{a_2}}{3} = \left[ V_a + V_b + V_c \right] \left( \frac{1}{3} \frac{1}{q} \right) + \frac{1}{q} \left[ V_a + V_b + V_c \right]

\frac{V_{a_2}}{3} = \frac{2}{18} \left[ V_a + V_b + V_c \right] + \frac{1}{q} \left[ V_a + V_b + V_c \right]

\frac{V_{a_2}}{3} = \frac{q \cdot V_{a_1} - V_{a_1}}{3}

\frac{V_{a_2}}{3} = \frac{q \cdot V_{a_1} - V_{a_1}}{3}

\frac{V_{a_2}}{3} = \frac{q \cdot V_{a_1} - V_{a_1}}{3}
\[ V_{o2} = A \left( V_{o1} + V_b + V_0 \right) - B \left( V_{o1} + V_b + V_0 \right) \]

\[ V_{o2} = 0 \]

**Q49** The output of the circuit on the right will be:

(a) 1V  
(b) 11V  
(c) -10V  
(d) 0V

**Solution**

It is voltage follower

\[ V_o = 1V \]

**Q54**
Since it is an inverting amp, so it inverses input so it is corrected.

There is no negative feedback so virtual short concept can not cancelled so voltage gain $A \approx \frac{1}{R}$. 

8. Calculate the voltage gain:

$I_1 = I_2$

$V_{o_2} = V_2 = \frac{v_2 - v_1}{R}$
\[ V_{02} = 2V_2 - V_1 \]

\[ I_2 = I_3 \]

\[ \frac{V_2 - V_1}{R} = \frac{V_1 - V_{01}}{R} \]

\[ V_{01} = 2V_1 - V_2 \]

**Note:** Here it is a differential Amp.

\[ V_0 = \left( V_{01} - V_{02} \right) \frac{R_6}{R_1} \]

\[ V_0 = \frac{1}{2} \left( 3V_1 - 3V_2 \right) \frac{R_6}{R_1} \]

\[ = 3 \left( V_1 - V_2 \right) \frac{R_6}{R_1} \]

\[ \frac{V_0}{V_1 - V_2} = 3 \frac{R_6}{R_1} \]

\[ \begin{align*}
\frac{V_0}{(V_1 - V_2)} & = 3 \\
\frac{R_6}{R_1} & = \frac{R_1}{R} = \frac{R}{R} 
\end{align*} \]

OR
\[ (1 + \frac{R_6}{R}) \left( \frac{R_6}{R_1} \right) \]

\[ \therefore R_6 = R \]

So

\[ (1 + 2) \frac{1}{1} = 3 \cdot \text{Ans} \]

Q37

\[ +10V \]

\[ V_{in} \]

\[ +5V0 \]

\[ 4k \Omega \]

\[ 1k \Omega \]

\[ -10V \]

\[ V_{out} \]
For the given circuit diagram calculate the voltage $V_o$.

\[ V_i = \frac{V_{in}}{R} = I_o e^{\frac{V_i}{kT}} \quad \{ I_D = I_o e^{\frac{V}{kT}} \} \]

\[ V_i = I_o e^{\frac{V_i}{kT}} \quad \text{if} \quad V_o = 0 - V_o \quad \Rightarrow \quad V_i = -V_o \]

\[ V_i = I_o e^{-\frac{V_o}{kT}} \]

\[ \frac{V_i}{I_o} = \frac{-V_o}{kT} \]

\[ \ln \frac{V_i}{I_oK} = \frac{-V_o}{kT} \]

\[ V_o = -kT \ln \frac{V_i}{I_oK} \]

So it is a logarithmic amplifier.
Q. Calculate \( V_0 \).

\[ I_1 + I_2 = 0 \]

\[ I_0 e^{\frac{V_0}{kT}} + \frac{V_0 - 0}{R} = 0 \]

\[ I_0 e^{\frac{V_0}{kT}} = -\frac{V_0}{R} \]

\[ V_0 = -I_0 R e^{\frac{V_0}{kT}} \]

\[ \therefore V = V_i - 0 \]

\[ V_i = V_i \]

So it is an exponential amplifier or antilogarithm amplifier.

Q. For the given circuit diagram determine the current in terms of \( V_i \).
\[ I_L = \frac{V_{an} - 0}{R_1} = \frac{V_{an}}{R_L} \]

By K.C.E.
\[ \frac{V_i - V_{an}}{R} + \frac{V_o - V_{an}}{R} = \frac{V_{an}}{R_L} \]
\[ \frac{V_i}{R} - \frac{V_{an}}{R} + \frac{V_o}{R} - \frac{V_{an}}{R} = \frac{V_{an}}{R_L} \]
\[ \frac{V_i}{R} + \frac{V_o}{R} = \frac{V_{an}}{R_L} + \frac{2V_{an}}{R} \]
\[ \frac{V_i + V_o}{R} = V_{an} \left( \frac{1 + \frac{2}{R_L}}{R_L} \right) \]
\[ V_i + V_o = V_{an} \left[ \frac{R}{R_L} + 2 \right] \]

Again by K.C.E.
\[ I_3 + I_4 = 0 \]
\[ 0 = \frac{V_m}{R} + \frac{V_o - V_{an}}{R} \]
\[ \boxed{V_o = 2V_{an}} \]

From (1)
\[ V_i + 2V_{an} = V_{an} \left[ \frac{R}{R_L} + 2 \right] \]
\[ \boxed{V_o = \frac{V_i + 2V_{an}}{R_L}} \]
So, \( I_L = \frac{V_i}{R_L} \)

\[ = V_i \cdot \frac{R_L}{R} \]

\[ I_L = \frac{V_i}{R} \]

2. Calculate \( I_L \) in terms of \( V_i \).

\[ I_1 + I_2 = I_L \]

\[ \frac{V_o}{R} + \frac{V_0 - V_i}{R} = \frac{V_{in} - 0}{R_L} \]

\[ - \frac{V_{in}}{R} + \frac{V_0}{R} - \frac{V_{in}}{R} = \frac{V_{in}}{R_L} \]

\[ \frac{V_0}{R} = \frac{V_{in}}{R_L} + \frac{2}{R} \frac{V_{in}}{R} \]

\[ \frac{V_0}{R} = V_{in} \left[ \frac{1}{R_L} + \frac{2}{R} \right] \]

\[ V_0 = V_{in} \left[ \frac{R}{R_L} + 2 \right] \]
\[ I_L = \frac{V_{in} - V_o}{R_L} = \frac{-V_i R_L}{R_L} \]

\[ V_o = AV_i \]

*Note:*
\[ V_s - \beta AV_i = V_i \]
\[ V_s = V_i + \beta AV_i \]
\[ V_s = V_i \left[ 1 + A \beta \right] \]
\[ V_i = \left( \frac{V_s}{1 + A \beta} \right) \]
\[ V_o = A \frac{V_s}{1 + A \beta} \]

\[ \frac{V_o}{V_s} = \frac{A}{1 + A \beta} \]

*Negative feedback is used to decrease the gain or provide gain in the controlled manner, the controlling parameter is \((1+ A \beta)\).*

When \( \beta = \text{Feedback factor} \).

\[ \text{Ideal} \]

\[ \frac{V_o}{V_{in}} = 1 + \frac{R_6}{R_1} \quad \text{for } A_{01} = \infty \]

\[ \frac{V_o}{V_{in}} = \frac{-R_6}{R_1} \quad \text{for } A_{01} = \infty \]
If gain is not infinity:

\[
\frac{V_o}{V_{in}} = 1 + \frac{R_6}{R_1}, \quad \frac{V_o}{V_{in}} = -\frac{R_6}{R_1}
\]

\[
\frac{V_o}{V_{in}} = 1 + (1 + \frac{R_1}{R_1})A_{OL} \quad \frac{V_o}{V_{in}} = 1 + \left(1 + \frac{R_6}{R_1}\right)A_{OL}
\]

**Question:** For the given circuit diagram calculate the closed loop voltage gain if open loop gain \( A_{OL} = 50 \) \( \text{V/\text{V}} \).

\[
A_{OL} = 50
\]

\[
\frac{V_o}{V_{in}} = \frac{-R_6}{1 - (1 + \frac{10k}{1k})} = \frac{-R_6}{1 - \frac{10}{1}} = \frac{-R_6}{50}
\]

\[
\frac{V_o}{V_{in}} = \frac{-10}{1 + \frac{11}{50}} = \frac{-500}{61}
\]

\[
\frac{V_o}{V_{in}} = -0.196 \quad \text{Ans}
\]
Positive Feedback Op-Ampifier

The basic circuit diagram is used for positive feedback, it is a Schmitt trigger or a square wave generator also called as regenerative comparator. The basic operation of positive feedback is similar to open loop condition.

\[ V_i \rightarrow \rightarrow + \rightarrow V_o \]

\[ V_i - V_o = \frac{V_0 - V_2}{R_2} = 0 \]

\[ I_1 + I_2 = 0 \]

\[ 0 = \frac{V_2}{R_1} + \frac{V_o - V_2}{R_2} \]

\[ \frac{-V_2}{R_1} - \frac{V_2}{R_2} = \frac{-V_0}{R_2} \]

So, \[ V_o = \frac{V_2}{R_2} \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \]

\[ V_2 = \frac{R_1R_2 V_o}{(R_1 + R_2)} \]
\[
\frac{v_0}{v_1} = \frac{(R_2 + R_1)}{R_1 \cdot R_2}
\]

\[
v_2 = \frac{v_0 R_1}{(R_1 + R_2)}
\]

**Case I:** 
\[v_2 > v_i \Rightarrow v_0 = +V_{\text{sat}}\]

\[
v_2 = \frac{+V_{\text{sat}} \cdot R_1}{R_1 + R_2} = V_{\text{UT}} = \text{Upper Threshold voltage.}
\]

**Case II:** 
\[v_2 < v_i \Rightarrow v_0 = -V_{\text{sat}}\]

\[
v_2 = \frac{-V_{\text{sat}} \cdot R_1}{R_1 + R_2} = V_{\text{LT}}
\]

Here \[\beta = \frac{R_1}{R_1 + R_2}\] is feedback factor.
2.5 Feedback factor ($\beta$) of circuit $\omega$.

(a) 0.33  (b) 0.67  (c) Data is insufficient

0.08
2. For the given circuit diagram, calculate overall input resistance and overall output resistance with feedback shown in figure.

\[ V_i \quad o \quad V_o \]

\[ A_{0L} = 10^6 \]
\[ R_{in} = 10 \, k \, \Omega \]
\[ R_0 = 2k \]
\[ R_i^1 = 9 \]
\[ R_o^1 = 9 \]

\[ \beta = \frac{R_i^1}{R_i^1 + R_2} \]
\[ = \frac{2k}{2k + 3k} = \frac{2k}{5k} = 0.4 \]
\[ \beta = 0.4 \]

\[ R_{in}^1 = R_{in} \times (1 + \beta) \]
\[ \Rightarrow \]
\[ R_{in}^1 \rightarrow \infty \]

\[ R_{o}^1 = \frac{R_o}{1 + \beta} \]
\[ \Rightarrow \]
\[ R_o^1 \rightarrow 0 \] for op-amp

So, \[ R_{in}^1 = 10 \, k \times [1 + 10^6 \times 0.4] = 10 + 10^6 \times 10^6 \times 2 \]
\[ = (10 + 9 \times 10^6) \]

\[ R_{o}^1 = \frac{2k}{1 + 10^6 \times 0.4} = \frac{2}{1 + 10^6 \times 2} \]
\[ V_2 = \frac{V_0 R_1}{R_1 + R_2} \]

\[ V_2 \geq V_{\text{in}} \quad V_0 = +V_{\text{sat}} \]

\[ V_2 = +V_{\text{sat}} \frac{R_1}{R_1 + R_2} = V_{UT} \]

\[ V_2 < V_{\text{in}} \quad V_0 = -V_{\text{sat}} \]

\[ V_2 = -V_{\text{sat}} \frac{R_1}{R_1 + R_2} = V_{LT} \]

Transfer characteristics of feedback Op-amp:
\[ V_H = V_{UT} - V_{LT} \]

\[ V_H = \text{Hysteresis Voltage} \]

Q: for the given circuit diagram, draw the transfer characteristic and hence calculate hysteresis voltage.

\[ V_{o2} = \frac{V_o R_1}{R_1 + R_2} \]
\[ = \frac{V_o \times 1K}{1K + 2K} \]
\[ V_{o2} \leq \frac{V_o}{3} \]

\[ V_{UT} = V_{o2} = +\frac{V_{sat}}{3} = +\frac{15}{3} = +5\ V \]

\[ V_{LT} = V_{o2} = -\frac{V_{sat}}{3} = -\frac{15}{3} = -5\ V \]
\[ V_H = 5 - (-5) = 10 \text{V} \]

\[ V_H = 10 \text{V} \]

\[
\begin{array}{c}
N_{\text{op}} \quad \text{V}_{\text{in}} \\
0 \quad \text{V}_{\text{out}} \\
-5 \quad +5 \\
\end{array}
\]

\[ I_1 + I_2 = 0 \]

\[
\frac{1 - V_2}{\frac{8}{19} + \frac{V_0 - V_2}{950}} = 0
\]

\[
I = \frac{V_0}{95} = \frac{V_2}{51} + \frac{V_2}{5100}
\]

\[ 1 - V_2 + \frac{V_0 - V_2}{19} = 0 \]

\[ Q_0 \cdot V_2 = \frac{V_0 + 19}{19} \]
\[ V_2 = \frac{V_0 - 19}{20} \]
\[ V_{UT} = \frac{-10 + 19}{20} = \frac{9}{20} \]
\[ V_{LT} = \frac{-10 + 19}{-20} = \frac{9}{20} \]
\[ V_H = V_{UT} - V_{LT} = \frac{9}{20} - \frac{9}{20} = \frac{9}{20} = 1 \]
\[ V_H = 1 \text{V} \]

Draw for the given circuit diagram calculate hysteresis voltage.

For the given circuit diagram, calculate the hysteresis voltage.

\[ V_2 = \frac{V_0 R_1}{R_1 + R_2} \]
\[ V_0 = \frac{V_0 R_1}{R_1 + R_2} \]

When \( V_2 > V_{in} \), \( V_0 = +V_{sat} = +15 \)\(^{-}\)

\[ V_2 = \frac{15}{3} = +5 \text{ V} \]

\[ V_0 = +5 \text{ V} \]

When \( V_2 < V_{in} \), \( V_0 = -V_{sat} = -15 \)

\[ V_2 \cdot V_{LT} = -15 \cdot \frac{R_1}{R_1 + R_2} \]

\[ V_{LT} = -15 \cdot \frac{1k}{1k + R_2} \]

\[ V_{LT} = -15 \cdot \frac{1k}{9k} = -1.67 \text{ V} \]

\[ V_H = 0.75 \]

2. Calculate output voltage \( V_0 = ? \)
Q1: Calculate the current through each branch.

Q2: For the given circuit diagram determine the output voltage.
Characteristic Parameters of Op-Amp:

(i) Open Loop Voltage Gain \( A_{ol} = \infty \)
(ii) Input Resistance \( R_i = \infty \)
(iii) Output Resistance \( R_o = 0 \)
(iv) Slew Rate \((SR)\):

\[
SR = \frac{dV_o}{dt}
\]

Rate of change of output voltage with respect to time is called as "Slew Rate".

\[
SR = \frac{dV_o}{dt} \max_{V_o \to \infty}
\]

SI Unit:

\[
\text{Volt/sec}
\]

Standardized Unit:

\[
\text{Volt/\mu s}
\]

(v) Output Offset Voltage:\( V_{00} \)

Whenever both the inputs are grounded, some output voltage is available at
The output that is called Output offset voltage.
Ideal value of Output offset voltage is zero.

Input offset voltage : \( \{ V_{io} \} \) - To reduced the effect of output offset voltage the voltage used at the input is called as input offset voltage.

Vii) CMRR (Common Mode Rejection Ratio):

\[
\text{CMRR} = \frac{A_d}{A_c}
\]

\( A_d \) = differential gain
\( A_c \) = common gain or noise gain.

Ideal value of CMRR = \( \infty \)

Noise is send for -ve or +ve terminal of Op-amp.
It is used to reject the effect of noise.

It is defined as noise rejecting ability of the system.

OR

The ratio of the differential gain \( A_d \) and \( A_c \) of common mode gain.

\[
\text{(CMRR)}_{dB} = 20 \log \left( \frac{A_d}{A_c} \right)
\]
A voltage follower circuit having input voltage \( V_{in} = V_m \sin \omega t \). Calculate the maximum frequency at which slow rate becomes maximum.

\[
\begin{align*}
\text{SR} &= \left. \frac{dV_o}{dt} \right|_{\text{max}} \\
&= \left. \frac{d\left(V_m \sin \omega t\right)}{dt} \right|_{\text{max}} \\
&= V_m \omega \cos \omega t \\
\end{align*}
\]

At maximum, \( \cos \omega t = 1 \)

\[
\begin{align*}
\text{SR} &= V_m \omega \\
\text{SR}_{\text{max}} &= \frac{V_m \omega}{V_m} \\
\omega_{\text{max}} &= \frac{\text{SR}_{\text{max}}}{V_m} \\
\text{SR}_{\text{max}} &= \frac{V_m \omega}{V_m} \\
\omega_{\text{max}} &= \frac{V_m \omega}{V_m} = \omega_{\text{max}}
\end{align*}
\]
PN Junction Theory

* Crystal Structure of p-type and n-type semiconductor:

Intrinsic pure (\(\sigma_{++}\))

- to increase \(\sigma\) doping performed

- n-type
- intrinsic + pentavalent
- impurity
  - 5 + 4
  - 8 + 1

- p-type
- intrinsic + trivalent
- \(9 + 3\)
- \(7 + 1\)
- Positive type semiconductor

N-type Semiconductor:

[Diagram of N-type semiconductor]

- P-type semiconductor:
R-type Semiconductor

Whenever a proper covalent bonding take place between a p-type and n-type semiconductor the resultant crystal is called as p-n junction diode.

"In an intrinsic semiconductor from one side p-type substance and another side n-type substance will diffuse the point at which they will meet will form a junction is called as p-n junction."
Once a p-n junction is formed, initial diffusion occurs from one region to another. After a certain amount of diffusion, a potential is created which opposes the further flow of charge carriers, hence called as barrier potential, or contact potential or build in potential separated by (Vb).

The region in which potential barrier created there is no free charge carriers hence called as depletion region. The value of contact potential can never be measured by ordinary voltmeter.

* Baising: - for the practical application of diode certain voltages are applied at both end, is called as “baising.”

Forward Biasing: - Under forward bias condition, the width of the depletion region decreases as applied voltage increases.
Under forward bias condition as the forward voltage increases, the current across the diode increases exponentially. The direction of current under forward condition will be from $+n$ to $p$ type.

The minimum voltage after which the current increases to the large amount is called as cut-in voltage or threshold voltage.

Under forward bias condition a capacitor will exist called as diffusion capacitor. Capacitance appears to be negligible because depletion layer is very thin.
DC Resistance & the Resistance under forward Bias Condition.

Res. linear characteristics: $V \propto I$

for both:

$V = R_1 I$

$\frac{\Delta V}{\Delta I} = R_1$

In straight line graph:

The selection gives value as $\frac{V}{I}$

for any circuit at a fixed voltage the circuit will operate at a fixed current that voltage & current will give the operating point of circuit.

dc means point analysis.
AC: When our curve is non-linear...

The AC analysis defines about neighbouring point.

AC Resistance:

\[ I = I_0 e^{\frac{\nu}{\eta N_T}} \]

or

\[ I = I_0 \left[ e^{\frac{\nu}{\eta N_T}} - 1 \right] = I_0 e^{\frac{\nu}{\eta N_T}} - I_0 \]

Very small so it is neglected.

So

\[ I = I_0 e^{\frac{\nu}{\eta N_T}} \]

\( \eta \) - Recombination factor.

If \( \eta \) (increase \( T \)) \( \Rightarrow \) width of depletion layer also increases.

\[ R_{ac} = \frac{dI}{dV} = \frac{1}{dV/dI} = \frac{I_0 - I_1}{V_n - V_i} = \text{slope} \]

\[ R_{ac} = \frac{1}{\text{slope}} \]

\[ R_{ac} = \frac{1}{d \left( I_0 e^{-\nu/N_T} \right)} \]
\[ \frac{d}{dv} \frac{I_{0}}{e^{V/nVT} - 1} = \frac{I_{0} e^{V/nVT}}{nVT} \]

\[ I = \text{forward current} \]

\[ V_{T} = \text{Thermal Voltage} \]

\[ R_{ac} = \frac{g_{m} V_{T}}{I} \]

\[ R_{ac} \approx \frac{g_{m} V_{T}}{I} \]

\[ \text{Recombination factor} \]

* Equivalent symbol of representation of p-n junction diode under forward bias condition:

* Reverse Biasing:

\[ V_{f} \approx 0.7 \text{ V} \]

\[ V_{f} = 0.7 \text{ V} \]

\[ V_{f} = 0.7 \text{ V} \]
Under reverse bias condition, the width of the depletion layer increases.

Under reverse bias condition, minority carriers cross the junction hence the current is because of minority carriers. It is very less (negligible).

Under reverse bias condition, a capacitance exists called transition capacitance $C_T$.

* Equivalent representation of reverse bias:
Q

for the given circuit diagram determine of

dynamic resistance: $R_{dc} = \frac{V_{ac}}{I} = \frac{6.5 \, V}{0.1 \, A} = 65 \, \Omega$

$-g_{mn} + I_{ok} = 0$

$J = \frac{V_{ac}}{I_{ok}} = 46 \, \text{mV}$

$K = \frac{V_{ac}}{I_{ok}} = 46 \, \text{mV}$

Ideal Case:

calculate dynamic resistance $R_{dc}$ and $g_{mn}$, voltage $V_{ac}$ and current $I_{ok}$.
Equivalent Circuit:

\[ -9V + V_0 = 0 \]

\[ V_0 = -9V \]

Current:

\[ -40 + I \times 10 = 0 \]

\[ I = 9 \text{mA} \]

Q. For the given circuit diagram, identify which of the diodes are under forward bias.

<table>
<thead>
<tr>
<th>Option</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a)</td>
<td>on</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>(b)</td>
<td>on</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>(c)</td>
<td>off</td>
<td>on</td>
<td>off</td>
</tr>
<tr>
<td>(d)</td>
<td>off</td>
<td>on</td>
<td>on</td>
</tr>
</tbody>
</table>
2. For the given circuit diagram determine the current $I_1$ and $I_2$.

$I_1 = 0$ (Because of reverse bias)

$90 + 90I_2 = 0$

$\boxed{I_2 = 2mA}$

$V_2 = \frac{90 \times 10}{2 \times 10} = 45V$

$V_1 = \frac{90 \times 10}{20} = 45V$

2. For the given circuit diagram determine $I_1$ and $I_2$.

$D_2$ is Reverse

$V_0, I_1 = 0$
for the given circuit diagram calculate $I_1, I_2$.
Hence identify which of the diodes are under forward bias.

$V = 6V$

$I_1$ is reverse bias so $I_1 = 0$

$5V + 10 \times 10 = 15V$

$10I = 10$

$I = 1mA$
for the given circuit diagram calculate I and Vo.

\[ V = 0 \] \quad \text{becoz \( V_0 \) is connected to ground} \]

\[ 10 \text{J} - 5 = 0 \]

\[ I = 0.5 \text{mA} \]

for the given circuit diagram assume all the diodes are forward biased, each diode having a current of 0.5 mA, calculate the value of \( R_1, R_2, R_3 \).
\[ I = \frac{V_f - V_0}{R} \]

\[ R = \frac{V_f - V_0}{I} = \frac{10 - 6}{0.5} \]

\[ R_1 = \frac{9}{0.5} \]

\[ R_2 = \]
Problem 1: For the given circuit diagram, determine output voltage and current across the circuit.

\[ -10 + 0.3 + V_0 = 0 \]
\[ V_0 = 9.7 \text{ V} \]

\[ 10 + 0.3 + I \times 10k = 0 \]
\[ I = \frac{9.7}{10k} = 0.77 \text{ mA} \]
\[ I = 0.77 \text{ mA} \]

Question 2: Calculate output voltage and current.

\[ \text{Given} \quad \text{Si} \]
\[ 10 \text{ V} \]
\[ 10 \text{ V} \]
\[
V_0 = 9 \text{V}
\]

\[
-10 + 0.3 + 0.7 + V_0 = 0
\]

\[
I = \frac{9}{10} \Rightarrow I = 0.9 \text{mA}
\]

2. Calculate output voltage and current.

When two diodes are in parallel, the diode which is having lesser cut in voltage will replace the diode of higher cut in voltage.
So equivalent circuit diagram.

\[ 10 + 0.3 + V_0 = 0 \]
\[ V_0 = 9.7 \text{V} \]

\[ -10 + 0.3 + 10I = 0 \]
\[ 10I = 9.7 \]
\[ I = \frac{9.7}{10} \]
\[ I = 0.97 \text{mA} \]

**Question:** for the given circuit diagram calculate the value of \( R_1, R_2, R_3 \) assume each diode is having a voltage drop of 0.6V and current across each diode is 0.5mA.
\[ V_1 = 5.4 \text{ V} \]
\[ V_2 = 0.6 \text{ V} \]
\[ R_1 = \frac{9.9 - 5.4}{0.5 \text{ m}\Omega} = \frac{4.5}{0.5} \]
\[ R_1 = 9 \text{ k} \]
\[ R_2 = \frac{5.9 - (-0.6)}{1 \text{ mA}} = \frac{6.5}{1} \]
\[ R_2 = 6 \text{ k} \]
\[ R_3 = \frac{-0.6 (-5)}{1.5} = \frac{3}{1.5} \]
\[ R_3 = 2.76 \text{ k} \]

2. For the given circuit diagram calculate current across each diode.
\[ I_D = \begin{cases} V_D^2 + 2V_D & \text{for } V_D > 0 \\ 0 & \text{for } V_D \leq 0 \end{cases} \]

\[-10 + I_D + V_D = 0\]

\[-10 + V_D^2 + 2V_D + V_B = 0\]

\[V_D^2 + 3V_D - 10 = 0\]

\[a_n^2 + 3a_n - 10 = 0\]

\[a_n = \frac{-3 \pm \sqrt{9 - 4\times1\times10}}{2\times1} = 5, -2\]

\[V_D = 5V\]
Wave Shaping Circuits:

Wave shaping circuits are classified as:

1. Clippers:
   These are used to cut the certain portion of waveform. Hence called as Slicers or Chopper or Clipper. If positive waveform is clipped so called as positive clipper. If negative portion is clipped then it is called negative clipper. If both operation is performed then it is called as double clipper. The basic circuit elements are register, diode.

2. Clampers:
   These are used to shift the waveform either towards positive or negative. If shift is towards the side called as positive clipper, otherwise negative clampers.

Basic circuit elements are capacitor, diode. In the clapper circuit addition of dc takes place hence shift occurs.
Shunt Clipping

Series Clipping

Diode and Op in Parallel

Shunt Clipping

Series Clipping

Diode and Op in Parallel

Clippers can be classified as:

1. Shunt
2. Series

Clippers:

405

Rectifiers:

3. Rectifiers

A rectifier is a device that converts AC to DC.
Draw the output waveform.

\[ V_i > 0 \Rightarrow \text{DFB} \]
\[ V_i < 0 \Rightarrow -V_i \text{ R.B} \]

Draw the output waveform.

\[ V_i > 0 \Rightarrow \text{DFB} \]
\[ V_i < 0 \Rightarrow \text{R.B} \]

Draw the off waveform.

\[ V_i \geq 3 \text{ (3V to 10)} \]
\[ V_i \leq 3 \text{ (2.9V to 10)} \]

\[ 10 \sin t \]
\[ R \text{ (few ohms)} \]
\[ V_0 \]
Draw the output waveform.

\[ V_i > 3 \ (3.1 \text{ to } 10) \ D\%B \]
\[ V_i < 3 \ (2.9 \text{ to } 10) \ D\%B \]

2. Draw the o/p waveform.

\[ V_i > -3 \ (2.9 \text{ to } 10) \ FB \]
\[ V_i < -3 \ (3.1 \text{ to } 10) \ R\%B \]
Q. Draw the output waveform.

\[ V_i \geq -3 \quad (2.9 \text{ to } 10) \]

\[ V_i \leq -3 \quad (3.1 \text{ to } 10) \]
Q1. For the given circuit, identify the Mod.

Mod - 10

Q2. For the given circuit diagram, identify the Mod?

This is up counter

Mod-3 up counter

Q3. Design a Mod-5 down counter.

\[ f_x = \overline{Q_3} Q_1 \]
Identify the Mod of the given circuit diagram.

This is a down counter.
Ans: Mod-5 down counter.

Identify the Mod of the given circuit diagram.

This is a down counter.
Ans: Mod-10 down counter.
For the given circuit diagram draw the o/p.

\[ V_i \geq 5 \rightarrow D_1 FB, D_2 RB \]
\[ V_i \leq 2 \rightarrow D_1 RB, D_2 FB \]
\[ 2 < V_i < 5 \]

\[ V_i \leq -5 \rightarrow D_1 FB, D_2 RB \]
\[ V_i \geq -2 \rightarrow D_1 RB, D_2 FB \]
\[ -5 < V_i < -2 \rightarrow D_1 FB, D_2 RB \]

Q. Draw the o/p waveform.
Q. Draw the output waveform.

\[ V_i > 5 \Rightarrow D_1 FB, D_2 RB \]
\[ V_i < 0 \Rightarrow D_1 RB, D_2 FB \]
\[ 0 < V_i < 5 \Rightarrow D_1 RB, D_2 RB \]

Q. For the given circuit diagram draw the O/P waveform.

\[ V_i > 0 \Rightarrow FB \]
\[ V_i < 0 \]
Q. Draw the o/p waveform.

\[ V_i \geq 0 \text{ DFB} \]
\[ V_i \leq 0 \text{ -R B} \]

Qn. Draw the o/p waveform?

\[ V_i < 3 \rightarrow \text{R B} \quad 0 \text{/p voltage} \]
\[ -10 + 3 + V_o = 0 \]
\[ V_i > 3 \rightarrow \text{FB} \]
\[ V_o = 7 \]

Qn. Draw the o/p waveform.

\[ V_i < 7 \rightarrow \text{R B} \]
\[ V_i > 7 \rightarrow \text{FB} \]
Draw the output waveform?
Clampers:
These are used to shift the level of the waveform by providing certain d.c. component. The basic circuit elements are capacitor and diodes.

\[
\begin{align*}
+V_m & \quad +V_c \quad +V_o = 0 \\
V_o &= V - V_c \\
V_c &= V_m
\end{align*}
\]

Case I:
- \( V = V_m \)
- \( V_o = 0 \)

Case II:
- \( V = -V_m \)
- \( V_o = -2V_m \)

Q. For the given circuit diagram draw the o/p waveform.
Q. For the given circuit diagram, draw the o/p waveform.

Q. Draw the o/p waveform.

Q. Draw the o/p waveform.
Zener Diode

Specially fabricated diode (only fabricated in Si) 
the doping level of Zener diode is very high as compared to ordinary diode.

Under forward bias condition it behaves as ordinary diode.

"The main application of Zener diode is to operate under reverse bias condition."

The application of Zener diode is to operate:

(i) Voltage Regulator
(ii) Voltage Reference.

Note: Si < Ge

Conductivity: \( \sigma_{\text{Si}} < \sigma_{\text{Ge}} \)

Leakage Current: \( I_{0 \text{ Si}} < I_{0 \text{ Ge}} \)

\( n \text{ Amp. order} \) \( \uparrow \)

*Si is not preferred over Ge*

Q. For the given diode circuit, draw the output waveform.

\[ V = 3 \text{V} \]

\[ I_0 \sin t \]
Under reverse bias condition before achieving breakdown voltage, the current across Zener diode is minimum, represented by broken wire.

Once the breakdown voltage achieved or crosses the breakdown voltage, Zener diode will maintain a constant voltage of breakdown voltage.

\[ V_{Z} \]

\[ I_{\text{min}} \ (\text{nKnee, Zener}) \]

\[ V \]

\[ I \]

---

Zener Diode as Regulator:

\[ + \]

\[ V_s \]

\[ - \]

\[ I \]

\[ R_L \]

\[ V_0 \]

\[ + \]

\[ - \]

\[ V_s + I R_L = 0 \]

\[ V_s = V_0 \]

\[ V_0 = V_s \]

The output voltage does not fluctuate because of variation in supply voltage or variation in load resistance, \( R_L \).

Equivalent symbol representation of Zener diode.
To maintain a constant output voltage, a zener diode connected parallel with the load shows that it maintains a constant output voltage.

\[
V_Z = V_Y = V_Z
\]

For the given circuit diagram, calculate output voltage?

\[
V_S = 6V \quad R_L = 6V
\]

Equivalent circuit diagram

\[
+ \quad 0.7 + 7 = V_0
\]

\[
\sqrt{V_0 = 7.7}
\]
Q. Calculate the output voltage?

\[ V_0 = 7.7 \text{ V} \]

Q. For the given circuit diagram calculate the output voltage.

\[ V_0 = 5 \text{ V} \]
Q. For the given circuit diagram, draw the output waveform.

Q. Draw the output waveform.

Q. Draw the output waveform.

It is too low so it is represented by broken wire.
Q. \textbf{Draw the o/p waveform.}

[Diagram of a circuit with a 10\sin t term and a 3V diode labeled as \(D_1\) and \(D_2\) creating a feedback loop.]

Q. \textbf{Draw the o/p waveform.}

[Diagram of a circuit with a 10\sin t term and a 4V diode labeled as \(D_1\) and \(D_2\) creating a feedback loop.]

\begin{itemize}
  \item For positive half cycle: Diode \(D_1\) in \(R_B\) less than 5V
  \item 0.105V
  \item Greater than 5V
\end{itemize}
2. Draw the op waveform

For +ve:

For -ve:

2. Draw the op waveform

For +ve:

Below 3V:

Above 3V:

For -ve:

For +ve
Two identical Zener diodes are placed back to back in series and are connected to a variable DC power supply. The best representation of the I-V characteristics of the circuit is:

[Diagram of a circuit with two Zener diodes in series, labeled as 3V and 7V.]

Q.1. Draw the O/P waveform.

[Hand-drawn waveform with positive and negative voltage levels indicated.]
For the given circuit diagram shown in figure a zener diode having a breakdown voltage of 7V connected parallel across load. If variation in the supply is 20 to 30V calculate the maximum and minimum load current. So that a knee current across the zener diode is.

\[ V_s = (20 + 30)V \]

\[ I = I_Z + I_L \]

\[ I_L = I - I_Z \]

\[ I_L = \frac{V_s - 7}{50} \]

\[ I_{max} = \frac{30 - 7}{50} = \frac{23}{50} = 0.46A = 460mA \]

\[ I_{min} = \frac{20 - 7}{50} = \frac{13}{50} = 0.26A = 260mA \]

So for 0:

\[ (I_L)_{max} = (460 - 5)mA = 455mA \]

\[ (I_L)_{min} = (260 - 5)mA = 255mA \]
Maximum Power Dissipation across Zener Diode

\[ P_z = V_z I_z \]

\[ (P_z)_{\text{max}} = V_z (I_z)_{\text{max}} \]

A zener-diode shown in figure has a knee current of 5 mA and a maximum allowed power.

\[ V = V_z \]

\[ I = I_z + I_L \]

\[ I_L = I - I_z \]

\[ (I_L)_{\text{max}} = 60 - I_z, \text{min} = 60 - 5 = 55 \text{ mA} \]
\[ I_2 = V_2 I_2 \]
\[ 6 \text{ V} = 6 I_2 \text{ max} \]
\[ I_2 = 5 \text{ mA} \]

\[
\left( I_2 \right)_{\text{max}} = 60 \text{ mA}, \quad \left( I_2 \right)_{\text{min}} = 60 - 0 \text{ mA}, \quad \left( I_2 \right)_{\text{min}} = 10 \text{ mA}.
\]

\[ 12 + 12 R + 5 = 0 \]
\[ R = \frac{12 - 5}{1} = \frac{7}{1} \]

\[ R = \frac{7}{1} \text{ ohms} \]

\[ I = I_2 + I_L \]
\[ \left( I \right)_{\text{max}} = 500 \text{ mA} \]
\[ \left( I \right)_{\text{min}} = 100 \text{ mA} \]
\[ R_{\text{max}} = \frac{7}{I_{\text{max}}} = \frac{7}{500 \text{ mA}} = 14 \Omega \]
\[ R_{\text{min}} = \frac{7}{I_{\text{min}}} = \frac{7}{100 \text{ mA}} = 70 \Omega \]

\[ R = \frac{70 \Omega}{3} \text{ ohms} \]
\[ 10 + I \cdot 50 + 6 = 0 \]

\[ I = \frac{9}{50} = 0.18m \text{A} \]

\[ -V + I \cdot R + 10 = 0 \]

\[ R = \frac{V - 10}{I} \]

\[ I = I_2 + I_L \]

\[ I = 1 + 10 \]

\[ I = 11 \text{mA} \]

\[ R = \frac{(V - 10)}{11 \text{mA}} = \frac{50 - 10}{11} = \frac{40}{11} = 3.6\Omega \]

\[ (R)_{\min} = \frac{30 - 10}{11} = \frac{20}{11} = 1.8\Omega \]
a. For the given circuit shown calculate the ratio of maximum and minimum power at the load. If the zener diode is having negligible leakage current and breakdown voltage = 10 V

\[ V = (5-20) V \]

\[ R_L = 1 k \Omega \]

**Case I:** \( V_i = 5 V \)

\[ V_{RL} = \frac{5 \times 1k}{0.5k} = \frac{50}{15} = 3.33 V \]

**Case II:** \( V_i = 20 V \)

\[ V_i = 20 V \]

\[ P = \frac{10^2}{1k} = 100 \text{ mW} \]

\[ P_{max} = \frac{100 \text{ mW}}{11 \text{ mW}} = 9.09 \]
for the half cycle

\[ V_i = 1.238 \text{ V} + 15^\circ \]

\[ V_i + 1.238 + 15^\circ = 0 \]

\[ V_i = 1.238 + 15^\circ \]
\[ I = I_{2} + I_{L} \]

Power \((P) = V_L I_L \Rightarrow I_L = \frac{P_L}{V_L} = \frac{150}{15} = 10 \text{ mA} \]

\[ (I_L)_{\text{max}} = 10 \text{ mA} \]

\[ P_{Z} = V_{Z} I_{Z} \]

\[ I_{Z} = \frac{P_{Z}}{V_{Z}} = \frac{800}{15} = 53.33 \text{ mA} \]

\[ (I_{Z})_{\text{max}} = 18.83 \text{ mA} \]

\[ I_{\text{max}} = (I_{Z})_{\text{max}} + (I_{L})_{\text{max}} = 18.83 + 10 = 28.83 \text{ mA} \]

\[ V_{i} = 23.8 \times 28.83 \text{ mA} + 15 \]

\[ (V_{i})_{\text{max}} = 20.5 \]

\[ I = I_{2} + I_{L} \]

\[ I = 0.110 \rightarrow 1.0 \text{ mA} \]

\[ V_{i} = 2.888 \times 15 \]

\[ V_{i} = 17.36 \]

So range of \( V_{i} \) is 17.5 V to 20.5 V \( \text{Ans} \)
\[
(25)_{10} \rightarrow (101101)_{2}
\]

Decimal to Other Conversion:

<table>
<thead>
<tr>
<th>Number System</th>
<th>Number of Digits</th>
<th>Number of Digits Used in any Number System</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decimal (16)</td>
<td>0 - 9</td>
<td></td>
</tr>
<tr>
<td>Octal (8)</td>
<td>0 - 7</td>
<td></td>
</tr>
<tr>
<td>Hexadecimal (16)</td>
<td>0 - 9</td>
<td></td>
</tr>
<tr>
<td>BCD (6)</td>
<td>0 - 1</td>
<td></td>
</tr>
<tr>
<td>Binary (2)</td>
<td>0 - 1</td>
<td></td>
</tr>
</tbody>
</table>

*Decimal to other conversion is the process of converting a number from one base to another. *
2. Identify the values of $R_1$ and $R_2$?

$(235)_{16} \approx (565)_{10} = (1068)_{16}$

(a) $12, 8$ (b) $16, 8$ (c) $8, 12$ (d) $8, 16$

2. Identify $\alpha \approx 9$

$(123)_{\alpha} = (12, \alpha)_{3}$

(a) $3$ (b) $-3$ (c) $5$ (d) None

If we found $\alpha$, we can't have $6$ in argument.

2. $(25.625)_{10} \rightarrow (\ ? \ )_{2}$

$(25)_{10} \rightarrow (11001)_{2}$

0.625

\[
\begin{array}{c|c|c|c}
\times 2 & 0.25 & 0.5 & 1.0 \times 2 \\
2.5 & 0 & 0 & 0 \\
\hline
\hline
\end{array}
\]

So $(25.625)_{10} \rightarrow (11001.101)_{2}$

2. $(25.625)_{10} \rightarrow (\ ? \ )_{2}$

$(25)_{10} \rightarrow (31)_{8}$
\[
\begin{align*}
\alpha &= 0.625 \\
\frac{\alpha}{\alpha} &= 0.625 \\
\text{So} \quad (25.625)_{10} &\rightarrow (81.5)_{8} \\
\end{align*}
\]

Other to decimal Conversion:

\[
\begin{align*}
\begin{array}{c}
1100 \downarrow \downarrow \downarrow \downarrow \\
2 \quad 2 \quad 1 \quad 0 \\
\end{array} \\
\rightarrow \quad (\quad )_{10}
\end{align*}
\]

\[
\begin{align*}
x^2 + 0 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4 \\
= 1 + 8 + 16 = 25 \\
(11001)_{2} &\rightarrow (25)_{10} \quad \text{Ans}.
\end{align*}
\]

\[
\begin{align*}
\begin{array}{c}
1101 \downarrow \downarrow \downarrow \downarrow \\
2 \quad 2 \quad 1 \quad 0 \\
\end{array} \\
\rightarrow \quad (\quad )_{10}
\end{align*}
\]

\[
\begin{align*}
x^2 + 0 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4 + 1 \times 2^5 + 0 \times 2^6 + 1 \times 2^7 \\
= 1 + 8 + 16 + \frac{1}{2} + \frac{1}{8} \\
25 + \frac{5}{8} = 25 + 0.625 \\
= 25.625 \\
(11001.101)_{2} &\rightarrow (25.625)_{10} \quad \text{Ans}
\end{align*}
\]
\[
\begin{align*}
(31)_{8} & \rightarrow (25)_{10} \\
1 \times 8^0 + 3 \times 8^1 &= 25 \\
1 + 24 &= 25 \\
(31)_{8} & \rightarrow (25)_{10} \\
(31.5)_{8} & \rightarrow (35.625)_{10} \\
1 \times 8^0 + 3 \times 8^1 + 5 \times 8^{-1} &= 35.625 \\
25 + \frac{5}{8} &= 25.625 \\
(12.3)_{8} &= (12.61)_{10} \\
\end{align*}
\]

\[3 \cdot 9^0 + 2 \cdot 9^1 + 1 \cdot 9^2 = a_n \cdot 9^0 + 2 \cdot 9^1 + 1 \cdot 9^2 \\
3 + 2a_n + a_n^2 = 9 + 6 + 9 \\
a_n^2 + 2a_n - 12 = 0 \\
\]

\[a_n = 3, -4 \]

It is not satisfied \(a_0\) option is none of these.
Octal Number System:

- Octal numbers can be represented in the range of 3-bit binary since the ranges are satisfied.

Hexadecimal Number System:

- Represented in terms of 9-bit binary. Hexadecimal can be

\[
\begin{align*}
0 & \rightarrow 0 \\
00 & \rightarrow 1 \\
01 & \rightarrow 2 \\
02 & \rightarrow 3 \\
03 & \rightarrow 4 \\
04 & \rightarrow 5 \\
05 & \rightarrow 6 \\
06 & \rightarrow 7 \\
07 & \rightarrow 8 \\
08 & \rightarrow 9 \\
09 & \rightarrow A \\
0A & \rightarrow B \\
0B & \rightarrow C \\
0C & \rightarrow D \\
0D & \rightarrow E \\
0E & \rightarrow F \\
0F & \rightarrow 10
\end{align*}
\]

Q.

Perform the conversion \((123.73)_8 \rightarrow (\_\_\_\_\_)_{16}\)

Solution:

\[
\begin{align*}
123 & \rightarrow 053 \quad 73 & \rightarrow FC
\end{align*}
\]

Q.

Find the minimum decimal equivalent of \((\_\_\_\_\_\_\_\_)_{16}\)

- We find minimum decimal equivalent

So \((1110131\, 11516)\) so for minimum we have 13.
9. Perform the addition \((127)_8 + (172)_8\)

\[
\begin{array}{c}
127 \\
172 \\
\hline
321 \\
\end{array}
\]

So = \((321)_8\) \text{ Ans}

10. The addition of two numbers are given as \(12.3 + 13.0 = (22.0)\). Perform the subtraction \(822 - 123\)

\[
\begin{array}{c}
12.3 \\
+13.0 \\
\hline
32.0 \\
\end{array}
\]

\[
\begin{array}{c}
822 \\
-123 \\
\hline
699 \\
\end{array}
\]

So = \((822)_4\) \text{ Ans}

11. Perform the multiplication \((1111)_2 \times (1111)_2\)

\[
\begin{array}{c}
1111 \\
\times1111 \\
\hline
1111 \\
1111 \\
\hline
11100001 \\
\end{array}
\]
**Compliment of Number System:**

In modern computer systems, two's (2's) complement representation is mainly used for performing arithmetic operations. It reduces the hardware requirement.

<table>
<thead>
<tr>
<th>Binary</th>
<th>2-1 1's</th>
<th>8 2's</th>
<th>10 1's</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>1</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>0001</td>
<td>1</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>0010</td>
<td>2</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>0011</td>
<td>2</td>
<td>12</td>
<td>10</td>
</tr>
<tr>
<td>0100</td>
<td>4</td>
<td>14</td>
<td>11</td>
</tr>
<tr>
<td>0101</td>
<td>4</td>
<td>14</td>
<td>10</td>
</tr>
<tr>
<td>0110</td>
<td>5</td>
<td>15</td>
<td>11</td>
</tr>
<tr>
<td>0111</td>
<td>5</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>1000</td>
<td>8</td>
<td>12</td>
<td>01</td>
</tr>
<tr>
<td>1001</td>
<td>8</td>
<td>12</td>
<td>01</td>
</tr>
<tr>
<td>1010</td>
<td>10</td>
<td>14</td>
<td>01</td>
</tr>
<tr>
<td>1011</td>
<td>10</td>
<td>14</td>
<td>01</td>
</tr>
<tr>
<td>1100</td>
<td>12</td>
<td>15</td>
<td>01</td>
</tr>
<tr>
<td>1101</td>
<td>12</td>
<td>15</td>
<td>01</td>
</tr>
<tr>
<td>1110</td>
<td>13</td>
<td>15</td>
<td>01</td>
</tr>
<tr>
<td>1111</td>
<td>13</td>
<td>15</td>
<td>01</td>
</tr>
</tbody>
</table>

In any number system in general base $\gamma$ then there exist two types of compliment -

1. $(\gamma-1)'s$ Compliment
2. $\gamma's$ Compliment

**Example**: Calculate 1's Compliment of 1010.

**Solution**

1. **1's Compliment**: Flip all the bits of 1010 to get 0101.

To calculate $(\gamma-1)'s$ Compliment, select maximum digit of that no. system and subtract each and every bit with that maximum value. The result is $(\gamma-1)'s$ Compliment.
Q. 10's

Find the F's Compliment of (3, 2, C, A)?

\[
\begin{align*}
F & F F F f \\
3 & 2 & C & A \\
\hline
C & D & 3 & 5 & \quad \text{F's Compliment.}
\end{align*}
\]

\[\text{To Calculate Y's Compliment from (X-1)'s Compliment add 1 at least significant bit (LSB).}\]

\[
\begin{align*}
10 & 10 \\
\text{First time} & 0 & 1 & 0 & 1 \\
\text{Second time} & 1 & 0 & 1 & 0
\end{align*}
\]

In any number system two times \((X-1)'s\) Compliment produces the same result.

\[
\begin{align*}
1's & - 0 & 1 & 0 & 1 \\
2's & - 0 & 1 & 1 & 0 \\
1's & - 1 & 0 & 0 & 1 \\
9's & + 1 & 0 & 1 & 0
\end{align*}
\]

\[
\begin{align*}
9 & 9 & 9 \\
6 & 7 & 9 & 8 & \quad 10 \\
\hline
3 & 2 & 0 & 1 & \quad \text{F's Comp. first time.}
\end{align*}
\]

\[
\begin{align*}
9 & 9 & 9 \\
3 & 2 & 0 & 1 \\
\hline
6 & 7 & 9 & 8 & \quad \text{F's Comp. second time.}
\end{align*}
\]

\[
\begin{align*}
1's & - 6 & 7 & 9 & 7 \\
2's & - 3 & 2 & 0 & 2 \\
\hline
2's & - 6 & 7 & 9 & 8
\end{align*}
\]
"In any no. system in general two times either (\(y-1\))'s Complement or 1's Complement produces same result."

**Signed Magnitude Representation:**

- MSB = 1 = No = \(-V\)
- MSB = 0 = No = \(+V\)

In an \(n\)-bit binary representation MSB will give sign. If MSB = 1 \(\Rightarrow\) No = \(-V\)

- MSB = 0 \(\Rightarrow\) No = \(+V\)

Rest \((n-1)\) bit will give the magnitude of the number.

<table>
<thead>
<tr>
<th>3-bit binary</th>
<th>Sign</th>
<th>Magnitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>+0</td>
<td>0</td>
</tr>
<tr>
<td>0 0 1</td>
<td>+1</td>
<td>1</td>
</tr>
<tr>
<td>0 1 0</td>
<td>+2</td>
<td>2</td>
</tr>
<tr>
<td>0 1 1</td>
<td>+3</td>
<td>3</td>
</tr>
<tr>
<td>1 0 0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1 0 1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>1 1 0</td>
<td>-2</td>
<td>-2</td>
</tr>
<tr>
<td>1 1 1</td>
<td>-3</td>
<td>-3</td>
</tr>
</tbody>
</table>

The disadvantage of sign magnitude is quick representation of \(+0\), \(-0\) require excess (large) memory space. Hence hardware requirement increases.

Note: Complement of any number system are only calculated for \(-ve\) numbers.
Complement's advantage is 2's Complement with 0 removed.
Range of representation also increases.

Range of Representation of sign magnitude and 2's Complement:

Range: -3 to +3
\[-[2^{(3-1)}] \text{ to } +[2^{(3-1)}]\]

For n bit
\[-[2^{(n-1)}] \text{ to } +[2^{(n-1)}]\]

Range of Rep. of 2's 2's Complement:
\[-[2^{(n-1)}] \text{ to } +[2^{(n-1)}]\]

Find the 2's Complement of \((-17)_{10}\).

\[
\begin{array}{c}
11111 \\
10001 \\
1's \\
01110 \\
1 \\
2's \\
01111
\end{array}
\]

For sign (for -ve sign use 1)

So \((-17)_{10} = (101111) \leftrightarrow 2's \text{ Comp.}\)

Find the 2's Complement of \((-2)_{10}\)

\[
\begin{array}{c}
10 \\
11 \rightarrow 0 \\
10 \rightarrow (110) \leftrightarrow 2's \text{ Comp.}
\end{array}
\]
Q. Repeat the previous quiz for 6-bit Comp.

\[ (-2)_{10} \]

1's \( \overline{1110} \)

+ 1

2's \( \overline{1110} \)

\[ \text{Since in previous quiz} \quad (-2)_{10} = 110 \]

\[ \overline{111} \quad \boxed{110} \]

\[ \text{Sign bit} \]

Note:
Whenever it is required to represent the complement of any no. system by using additional bits, copy the sign bit to the additional places.

Q. Find the 2's Complement of \( (+2)_{10} \)

\[ (+2)_{10} \]

0 \( \overline{10} \)

So \( (010)_{2} \) is

Q. Repeat the previous quiz use 6-bit representation.

\[ (+2)_{10} \]

0 \( \overline{10} \)

for 6-bit \( \overline{00010} \)

So \( (00010)_{6} \)
Weighted and Unweighted Code:

**Weighted Code:** In the number system representation, each and every bit is assigned by using significant powers positions. Such code representation is called Weighted Code.

If the codes are represented in an arbitrary manner in which each and every bit does not have significant bit are called as Unweighted Code.

**Example:**

Weighted BCD Code

<table>
<thead>
<tr>
<th>Decimal Code</th>
<th>BCD Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 4 2 1</td>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>2 1 2 1</td>
<td>0 0 1 1 1</td>
</tr>
<tr>
<td>5 2 1 1</td>
<td>0 1 0 0 0</td>
</tr>
<tr>
<td>3 3 2 1</td>
<td>1 1 1 0 0</td>
</tr>
</tbody>
</table>

Unweighted Gray

<table>
<thead>
<tr>
<th>Excess - 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>0 0 1 1 1</td>
</tr>
<tr>
<td>0 1 0 0 0</td>
</tr>
<tr>
<td>1 1 1 1 1</td>
</tr>
</tbody>
</table>

**Self-Complementary**

- BCD Code:

<table>
<thead>
<tr>
<th>Decimal Code</th>
<th>BCD Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 4 2 1</td>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>2 1 2 1</td>
<td>0 0 1 1 1</td>
</tr>
<tr>
<td>5 2 1 1</td>
<td>0 1 0 0 0</td>
</tr>
<tr>
<td>3 3 2 1</td>
<td>1 1 1 0 0</td>
</tr>
</tbody>
</table>
By calculation of 9's Compliment the resultant also gives 1's comp. Such codes are also called as Self Complementary Codes. For example, 5211, 8221, 2421, 8421 is a non-self Complementary Code.

**Excess-3 Code:** Excess-3 represents values from 0 to 9, but by adding 3 (0 to 9+3) to each value.

<table>
<thead>
<tr>
<th>8421</th>
<th>Excess-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0011</td>
</tr>
<tr>
<td>0001</td>
<td>0100</td>
</tr>
<tr>
<td>0010</td>
<td>0101</td>
</tr>
<tr>
<td>0011</td>
<td>0110</td>
</tr>
<tr>
<td>0100</td>
<td>0111</td>
</tr>
<tr>
<td>0101</td>
<td>1000</td>
</tr>
<tr>
<td>0110</td>
<td>1001</td>
</tr>
<tr>
<td>0111</td>
<td>1010</td>
</tr>
<tr>
<td>1000</td>
<td>1011</td>
</tr>
<tr>
<td>1001</td>
<td>1100</td>
</tr>
</tbody>
</table>

Something leakage.
**B.J.T.** - Bipolar junction transistor

**Emitter**: The function of emitter is to supply majority carriers. Doping of emitter must be very high.

**Collector**: The collector is used to collect all the majority carriers supplied by emitter. The doping of collector must be comparatively less w.r.t. to emitter.

**Base**: Base is also called as transit region through which majority carriers reach to collector. Width of the base must be as smaller as possible. Base will be having least doping.

In any transistor there exist two junctions:

1. \(E_E / E_e\)
2. \(C_E / C_e\)

The main purpose of transistor is to operate as amplifier.

Because transistor is costly so it is used as amp.

Diode is less costly so it is used as a switch.
Configuration of Transistor:

Common Base Configuration:

Common Emitter Configuration:

Common Collector Configuration:
Identify the configuration?

Common Collector Configuration

\[ \beta = \frac{I_C}{I_B} \]

\[ \alpha = \frac{I_C}{I_E} \]

Here \( \alpha, \beta, \gamma \) are current gains.
\[ I_C = \alpha I_E + I_0 \]

\[ I_C = I_{CO} = I_{CBO} = \alpha I_E + I_0 \]

\[ I_0 = \text{leakage current} \]

\[ I_E = I_B + I_C \]

Equation 1: divide by \( I_C \)

\[ \frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C} \]

\[ \frac{1}{\alpha} = \frac{1}{\beta} + 1 \]

\[ \frac{1}{\alpha} = \frac{1 + \beta}{\beta} \]

\[ \beta = \alpha(1 + \beta) = \alpha + \alpha \beta \]

\[ \beta - \alpha \beta = \alpha \]

\[ \beta (1 - \alpha) = \alpha \]

\[ \beta = \frac{\alpha}{1 - \alpha} \]

\[ I_C = \alpha (I_B + I_C) + I_{CO} \]

\[ I_C = \alpha (I_B + \alpha I_C) + I_{CO} \]

\[ (I_C + \alpha I_C) = \alpha I_B + I_C \]

\[ \Rightarrow \text{C.B.} \]
Common Emitter Configuration is having comparatively more current leakage current w.r. to Common base configuration by \((1+\beta)\) times.

\[
I_C = \frac{\alpha}{(1-\alpha)} I_B + (1+\beta) I_C0
\]

(1) \(I_E = I_B + I_C\)

(ii) \(\alpha = \frac{\beta}{1+\beta}\)

(iii) \(I_C = \alpha I_E + I_C0\)

(iv) \(I_C = \beta I_B + (1+\beta) I_C0\)

Q. A Transistor is excited by emitter current of 10m.A, \(\beta = 99\) leakage current \(I_C0 = 10\mu A\) find all other currents.

Soln

\[
I_C = \alpha I_E + I_C0
\]

\[
\alpha = \frac{\beta}{1+\beta} = \frac{99}{1+99} = \frac{99}{100}
\]

\[
I_C = 0.99 \times 10\mu A + 10\mu A
\]

\[
= 9.9\mu A + 0.01\mu A
\]

\[
I_C = 9.91\mu A
\]
A transistor is excited by base current of 20 μA. α = 0.99. Find all other currents.

Note: "If Configuration is not available then assume Common emitter Configuration."

\[ \beta = \frac{0.99}{1 - 0.99} = \frac{0.99}{0.01} = 99 \]

\[ I_C = \beta I_B = 99 \times 0.01 \text{ mA} \]

\[ I_E = I_B + I_C = 20 \times 10^{-3} \text{ mA} + 1.98 \text{ mA} = 2 \text{ mA} \]

Q. For the given circuit, sketch diagram calculate all the currents.

\[ I_C = 100 I_B \]

\[ \beta = 100 \] Here leakage current is not given, so assume ideally it is 0.

So \[ I_C = \beta I_B \]
Apply loop current:
\[-5 + I_B \times 50k + 0.7 = 0\]
\[I_B \times 50k = 5 - 0.7\]
\[I_B = \frac{5 - 0.7}{50}\]
\[I_B = 0.086 \text{ mA}\]

\[I_C = 100 \times 0.08 = 8.6 \text{ mA}\]
\[I_C = 8.6 \text{ mA}\]

\[I_E = I_B + I_C\]
\[= 0.086 + 8.6\]
\[I_E = 8.686 \text{ mA}\]

Apply loop:
\[-10 + I_C \times 3k + V_0 = 0\]
\[V_0 = 10 - I_C \times 3k\]
\[= 10 - 8.6 \times 3\]
\[= 10 - 25.8\]
\[V_0 = -15.8 \text{ V}\]

Q. Repeat the previous case by replacing emitter by 2kΩ.

So,
\[ I_c = \beta I_B + (1+\beta) I_{c0} \]

\[ I_{c0} = 0 \]

\[ I_c = \beta I_B \]

\[ I_c = 100 I_B \]

\[ I_B \times 50k + 0.7 + I_E \times 2k = 0 \]

\[ I_B \times 50k + (I_B + I_c) \times 2k = 9.8 \]

\[ I_B \times 50 + 2I_B + 2 \times 100I_B = 9.3 \implies I_B(50 + 2 + 200) \]

\[ I_B = \frac{9.3}{252} = 3.7 \times 10^{-6} \]

\[ I_B = 0.017 \text{mA} \]

\[ I_c = 100 \times I_B = 100 \times 0.017 \]

\[ I_c = 1.7 \text{mA} \]

\[ I_E = I_B + I_c \]

\[ I_E = 0.017 + 1.7 = 1.717 \]

\[ I_E = 1.717 \text{mA} \]

Apply loop for \( V_0 \):

\[-10 + I_c \times 3 + V_0 = 0 \]

\[ V_0 = 10 - I_c \times 3 = 10 - 1.7 \times 3 = 10 - 5.1 \]

\[ V_0 = 4.9 \text{V} \]
\[-10 + I_C \times 8K + V_{CE} + I_E \times 2 = 0\]

\[V_{CE} = 10 + 1.7 \times 3 - 1.717 \times 2\]
\[V_{CE} = 10 + 5.1 - 3.454\]
\[= \boxed{15} - 8.854\]

\[V_{CE} = 1.97V\]

Another Loop:
\[V_0 = V_{CE} + I_E \times 2\]
\[= 1.9 + 1.717 \times 2\]
\[= 1.9 + 3.934\]
\[V_0 = 9.834 \approx 9.9\]

\[V_0 = 9.9V\]

\[V_{CE} - V_{BE} - V_{CB} = 0\]
\[V_{CB} = V_{CE} - V_{BE}\]
\[V_{CB} = 1.97 - 0.7\]

\[V_{CB} = 0.9V\]

Significance of node around transistor

\[+V_{CE} - V_{BE} - V_{CB} = 0\]

Kirchhoff's Voltage Law.
\[ \alpha = 0.995, \quad I_{EB} = 10 \text{mA}, \quad I_{CBO} = 0.5 \text{mA}. \]

\[ I_{CEO} = \ ? \quad \Rightarrow \quad I_{CEO} = (1+\beta)I_C \]

\[ \beta = \frac{\alpha}{1-\alpha} \]

\[ \beta = \frac{0.995}{1-0.995} = \frac{0.995}{0.005} = 199 \]

\[ I_{CEO} = (1 + 199)I_C = 200 \times 0.5 = 100 \text{mA} \]

\[ I_{CEO} = 100 \text{mA} \]

**Q. 61** For the given circuit diagram.

\[ V_{BE} = 0.3 \]
\[ I_{CB} = 20 \text{mA} \]
\[ \alpha = 0.96. \]

**SOL**

\[ \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = \frac{0.96}{0.04} = 24 \]

\[ I_C = \beta I_B + (1+\beta)I_{CBO} \]
Applying loop:

\[-10 + I_B \times 100 + V_{BE} = 0\]

\[I_B = \frac{10 - 0.3}{100} = \frac{9.7}{100} = 0.097 \text{ mA}\]

\[I_B = 0.097 \text{ mA}\]

\[I_C = 24 \times 0.097 + 25 \times 0.2\]

\[I_C = 2.8 \text{ mA}\]

Apply loop by \(V_C\):

\[-10 + I_C \times 2.2 + V_C = 0\]

\[V_C = 10 - 2.0 \times 2.2\]

\[V_C = 10 - 6.16\]

\[V_C = 3.84 \text{ Volt}\]
* Early Effect: *

$I_B^+ \Rightarrow I_C^+ \Rightarrow I_E^+$

- Width of depletion layer increases when $V_{CB}$ increases.
- Reverse base width increases more in low doping side.

As collector to base voltage varies, effective base width varies in called base width modulation.

As collector to base voltage changes, the width of the base decreases so base current decreases.

* Common Base Configuration: *

Input Characteristics: $I_E^+$

$V_{CE} = V_0 + V$
"As \( V_{CB} \) increases, \( I_E \) increases as per Early Effect hence graph shift towards \( y \)-axis."

Output Characteristics:

\[ I_C = \alpha I_E \]
\[ \alpha \approx 0.99 \]
\[ I_C = I_E \]

Saturation Region (ON Switch)

Common Emitter Emitter Configuration:
Input Characteristics:

\[ V_{CE} - V_{BE} = V_{CB} \]
\[ V_{CE} = 0.7 = V_{CB} \]

Input characteristics is similar to forward characteristics of a pn-junction diode as \( V_{CB} \) increases graph shift towards x-axis.

Output Characteristics:

\[ I_C = \beta I_B + (1+\beta) I_{C0} \]

Ideally \( I_{C0} = 0 \)

\[ \beta = 100 \]

\[ I_B = 10 \mu A \]

\[ I_C = 1 mA \]

\[ V_{CE} = 0.7 = V_{CB} \]

\[ \uparrow V_{CE} = \uparrow V_{CB} + 0.7 \]

\[ \Rightarrow I_C = \beta I_B \]

Relation only applicable for active region.
Steps for Determination of Region of Operation:

Step I: Assume transistor is operating in saturation region.

<table>
<thead>
<tr>
<th>Saturation Voltage</th>
<th>Si</th>
<th>Ge</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BE, sat}$</td>
<td>0.0 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>$V_{CE, sat}$</td>
<td>0.2 V</td>
<td>0.1 V</td>
</tr>
</tbody>
</table>

Step II: Calculate $I_{B, sat}$ and $I_{C, sat}$ use only loop analysis (Don’t use $I_C = \beta I_B$).

Step III: Calculate $I_{B, min} = \frac{I_{C, sat}}{\beta}$

Current in active region.

- $I_{B, sat} > I_{B, min} \rightarrow$ Saturation Region
- $I_{B, sat} < I_{B, min} \rightarrow$ Active Region
- $I_{B, sat} = -ve \rightarrow$ Cut-off Region.

[Diagram of saturation and active regions]
Q. For the given circuit diagram identify the region.

Apply loop analysis:

\[-5 - V - I_{B, sat} \times 5 \Omega + V_{BE, sat} = 0\]

\[I_{B, sat} \times 5 \Omega = 5 - 0.8\]
\[I_{B, sat} = \frac{5 - 0.8}{5 \Omega} = 0.084 \text{ mA}\]

In another loop:

\[-10 + I_{C, sat} \times 3 \Omega + V_{CE, sat} = 0\]

\[I_{C, sat} = \frac{0.8}{3}\]
\[= 0.266 \text{ mA}\]

\[I_{\beta, min} = \frac{I_{C, sat}}{\beta} = \frac{0.266}{100}\]
\[= 0.00266 \text{ mA}\]

\[I_{\beta, min} = 0.0326 \text{ mA}\]

\[I_{\beta, sat} > I_{\beta, min}\]
\[0.01 > 0.0026\]

So it is in saturation region.
2. Find the region of operation of given transistor.

\[ V_{BE,\text{sat}} = 0.8\,V \]
\[ V_{CE,\text{sat}} = 0.2\,V \]
\[ \beta = 100 \]

\[-0.3\,V + I_{B,\text{sat}} \times 33.33 + V_{BE,\text{sat}} = 0 \]
\[ I_B \times 33.33 = -0.8 + 0.3\,V \]
\[ I_B = \frac{-0.5}{33.33} = -0.015\,\mu A \]

\[ I_B = -\text{ve} \]
So cut-off region.

2. For the given circuit diagram determine the region.

\[-5 + V_{B3\text{sat}} \times 5 + V_{BE,\text{sat}} + \frac{1}{\beta} \times 2K = 0 \]
\[ V_{BE,\text{sat}} = 0, 0.8\,V \]
\[ V_{CE,\text{sat}} = 0, 2\,V \]
\[ \beta = 100 \]
\[ -5 + I_{BSat} \times 50k + 0.3 + [I_{BSat} + I_{CSat}] \times k = 0 \]

\[ -5 + I_{BSat} \times 50k + 0.3 + [I_{BSat} + I_{CSat}] \times k = 0 \]

\[ I_{BSat} \times 50k + 0.3 \times k = 9.2 \]

\[ -10 + I_{CSat} \times 3k + V_{CEsat} + I_{ESat} \times k = 0 \]  \( \text{(1)} \times 5 \)

\[ -10 + I_{CSat} \times 3k + 0.2 + [I_{ESat} + I_{BSat}] \times k = 0 \]  \( \text{(2)} \)

\[ I_{BSat} \times 5k + I_{ESat} \times 5k = 9.8 \]  \( \text{(1)} \times 2 \)

\[ I_{BSat} + 260k + I_{CSat} \times 10k = 8.1 \]  \( \text{III} \)

\[ I_{BSat} \times 9k + I_{CSat} \times 10k = 19.6 \]  \( \text{IIV} \)

\[ I_{BSat} \times 25.6k = 9.4 \]

\[ I_{BSat} = \frac{9.4}{25.6k} \]

\[ I_{BSat} = 0.0683 \text{ mA} \]

So \( I_{CSat} \) from eqn (III):

\[ 0.0683 \times 260k + I_{CSat} \times 10k = 21 \]

\[ I_{CSat} = \frac{21 - 2.418}{10} = \frac{18.582}{10} \]

\[ I_{CSat} = 1.8582 \text{ mA} \]
Q. Assume the transistor is operating in saturation region and find the minimum value of \( \beta \). So that circuit produces stable operation in saturation region.

\[ \beta = 9 \]

\[ V_{BE \text{ sat}} = 0.8 \text{V} \]

\[ V_{CE \text{ sat}} = 0.2 \text{V} \]

\[ I_B = \frac{5 - 0.8}{50 \text{K}} \]

\[ = \frac{9.2}{50 \text{K}} \]

\[ I_{B \text{ sat}} = 0.0184 \text{mA} \]

\[ I_{C \text{ sat}} = \frac{10 - 0.2}{3 \text{K}} = 3.33 \text{mA} \]

\[ I_{C \text{ sat}} = 3.33 \text{mA} \]

\[ I_{B \text{ min}} = \frac{I_{C \text{ sat}}}{\beta} = \frac{3.33 \text{mA}}{\beta} \]

\[ \text{for } 0.0184 \text{mA} > \frac{3.83 \text{mA}}{\beta} \]

\[ \beta > 90 \]
Q. Repeat the previous question as \( \beta = 100 \) and calculate:

\[ I_{CB} = I_{B} + I_{C} \]

**Solution**

\[ I_{B, \text{sat}} = 0.089 \text{mA} \]

\[ -10 + I_{CSat} \cdot R_{C} + 0.2V = 0 \]

\[ -10 + I_{CSat} \cdot R_{C} + 0.2V = 0 \]

\[ I_{CSat} = \frac{10 - 0.2}{R_{C}} = 9.8 \]

\[ R_{C} = 3.266\Omega \]

\[ I_{B, \text{min}} = \frac{I_{CSat}}{\beta} \]

\[ I_{B, \text{min}} = \frac{9.8}{R_{C} \times 100} \]

\[ I_{CSat} > I_{B, \text{min}} \]

\[ 0.089 \text{mA} > \frac{9.8}{R_{C} \times 100} \]

\[ R_{C} > \frac{9.8}{0.089\times100} \]

\[ R_{C} > 11.12 \text{Ω} \] [Any]

---

Q. Assume the circuit is operating in saturation region. Determine the value of \( \beta \) for stable operations.

\[ -12 + I_{C} \times 3k \text{Ω} + 0.2V = 0 \]

\[ I_{C} = \frac{12 - 0.2}{3k} \]

\[ = 11.8 \text{mA} \]

\[ \frac{3.93\text{mA}}{8k} \]

Given \[ I_{B, \text{sat}} = 0.1 \text{mA} \]

\[ I_{B, \text{min}} = \frac{I_{CSat}}{\beta} = 3.93 \text{mA} \]

\[ \beta = ? \]
Condition of saturation

\[ I_{B\text{sat}} > I_{B_{\text{min}}} \]

\[ 0.1 \text{ m. m} > 3.9 \text{ mA} \]

\[ \frac{1}{p} > 89 \]

Fundamentals:

n-p-n

\[ I_B \]

\[ I_B + I_C = I_E \]

p-n-p

\[ I_E + I_B + I_C = 0 \]

\[ I_E = -(I_B + I_C) \]
Load Line: - A line drawn on the output characteristic is called as "load line".

![Circuit Diagram]

**Note:**

For larger values of $\beta$, $I_E = I_C$ and $I_B = 0$

\[
I_E = I_B + I_C
\]

\[
I_C = \beta I_E
\]

\[
I_B = \frac{I_C}{\beta}
\]

\[
\frac{1}{\beta} \approx 0 \text{ when } \beta \gg 1
\]

So, \[ I_C = I_E \]

Applying the loop:

\[-V_{cc} + I_c R_C + V_{CE} + I_E R_E = 0 \]

\[-V_{cc} + I_c R_C + V_{CE} + I_c R_E = 0 \]

\[
I_c \left( R_C + R_E \right) = -V_{CE} + V_{cc}
\]

\[
I_c = \frac{-V_{CE} + V_{cc}}{R_C + R_E}
\]

\[ I_c = m I_E + c \] (like $y = mx + c$)

\[ e_y \text{ of line.} \]
\[ V_{CE} = 0, \quad I_C = \frac{V_{CE}}{R_C + \beta R_E} \]

\[ V_{CC} \]  

\[ V_{CC} \]

\[ \beta \]

\[ \frac{15}{100} = 1.5 \text{mA} \]

**Q - Point**

A point selected on load line corresponding to a fixed voltage and fixed current at which transistor operates is called as operating point of the transistor, or Q-point or quiescent point.
If the operating point selected near saturation region or near cut-off region, then the upper portion of the waveform will be in saturation or cut-off where proper amplification is not found. Hence operating point selected approximately mid of the active region.

When current increases, voltage decreases. When voltage decreases, then current decreases.

\[ I_c = \beta I_b + (1+\beta)I_{co} \]

\[ I_c \uparrow \Rightarrow I_{co} \uparrow \Rightarrow V_c \downarrow \]

1. \( \beta \) mismatch
2. material mismatch
3. \( V_c \)

Once the operating point selecting at the center, it does not guarantees that it will remain at the center. It can change because of change in temp (Ico changes) hence Ic changes. Given by the expression:

\[ I_c = \beta I_b + (1+\beta)I_{co} \]
Replacement of transistor - mismatch

(iii) Replacement of transistor - Mismatch of material

turn cut in voltage changes.

* Stability factor: It is defined as a factor by how much collector current changes due to change in \( I_{co}, \beta \), Base-Emitter Voltage.

\[
S = \Delta I_c = \frac{\Delta I_c}{\Delta I_{co}} \quad \text{or} \quad \frac{\partial I_c}{\partial I_{co}}
\]

\[
S = \Delta \beta = \frac{\Delta I_c}{\Delta \beta} \quad \text{or} \quad \frac{\partial I_c}{\partial \beta}
\]

\[
S = \Delta V_{BE} = \frac{\Delta I_c}{\Delta V_{BE}} \quad \text{or} \quad \frac{\partial I_c}{\partial V_{BE}}
\]

"Ideal value of stability factor must be minimum \((\approx 0)\)."

\[
I_c = \beta I_B + (1 + \beta) I_{co} \quad \text{(1)}
\]

differentiate w.r.t. \( I_c \)

\[
\frac{\partial I_c}{\partial I_c} = \beta \frac{\partial I_B}{\partial I_c} + (1 + \beta) \frac{\partial I_{co}}{\partial I_c}
\]

\[
1 = \beta \frac{\partial I_B}{\partial I_c} + (1 + \beta) \frac{\partial I_{co}}{\partial I_c}
\]

\[
(1 + \beta) \frac{\partial I_{co}}{\partial I_c} = 1 - \beta \frac{\partial I_B}{\partial I_c}
\]
\[
\frac{\delta I_C}{\delta I_C} = \frac{(1-\beta) \frac{\delta I_B}{\delta I_C}}{(1+\beta)}
\]

\[
\frac{\delta I_C}{\delta I_C} = \frac{(1+\beta)}{(1-\beta) \frac{\delta I_B}{\delta I_C}}
\]

*Steps for calculating stability factor:
(i) Apply loop including input terminal
(ii) Calculate \( I_B \)
(iii) Find \( \frac{\delta I_B}{\delta I_C} \)

Q: For the given circuit diagram determine stability factor.

\[ I_B = \frac{V_{EE}}{R_C} \]

\[ \frac{\delta I_B}{\delta I_C} = \frac{1}{1+\beta} \]

\[ S = \frac{1+\beta}{1-\beta} \frac{\delta I_B}{\delta I_C} = \frac{1}{1+\beta} \]
Determine circuit factor

\[-V_{cc} + (I_c + I_B)R_C + I_e R_B + V_{BE} = 0\]

\[I_B (R_B + R_C) = V_{cc} - V_{BE} - V_{BR}\]

\[I_B = \frac{V_{cc} - V_{BE}}{R_B + R_C} - \frac{I_c R_C}{(R_B + R_C)}\]

\[\frac{dI_B}{dI_c} = -\frac{R_C}{R_C + R_B}\]

\[S = \frac{1 + \beta}{1 - \beta \left( -\frac{R_C}{R_C + R_B} \right)}\]

\[S = \frac{1 + \beta}{1 + \beta R_C} \frac{R_C}{R_C + R_B}\]

Q: And stability factor.

\[-V_B + I_B R_B + V_{BE} + I_e R_E = 0\]

\[-V_B + I_B R_B + V_{BE} + (I_c + I_B) R_B = 0\]

\[I_{R3} (R_{R3} + R_E) = V_B - V_{BE} - V_{BR} - \frac{I_c R_E}{R_B + R_E}\]

\[I_B = \frac{V_B - V_{BE}}{R_{R3} + R_E} - \frac{I_c R_E}{R_B + R_E}\]
\[
\frac{dI_B}{dI_C} = \frac{-RE}{R_B + RE} \quad \Rightarrow \quad S = \frac{1 + \beta}{1 + \beta \frac{RE}{R_B + RE}}
\]

\[-V_B + I_B R_B + V_B E - I_E R_E = 0\]

\[-V_B + I_B R_B + V_B E + (I_B + I_C) R_E = 0\]

\[
\frac{dI_B}{dI_C} = \frac{-RE}{R_B + RE}
\]

\[
S = \frac{1 + \beta}{1 + \beta \frac{RE}{R_B + RE}}
\]

*Stabilizing Circuit*:

To fix the operating point at the center the circuit used are called as stabilizing circuit.

Stabilizing Circuit

- Compensating circuit (logic)
- Biasing circuit (mathematics)
The diagram represents a circuit with the following elements:

1. **Resistor R**: The value of the resistor is marked as 2kΩ.
2. **Current Source Ie**: The current source is directed to the right.
3. **Transistor Q**: The transistor is labeled as Q1.
4. **Capacitor C**: The capacitor is marked as 100μF.
5. **Diode D**: The diode is labeled as D1.
6. **Voltage Source V**: The voltage source is connected to the right side of the circuit.

The circuit diagram shows a basic electrical circuit with a diode connected in parallel with a resistor and a capacitor. The diode is likely used to control the flow of current based on the voltage across it.

**Mathematical Description**:

- **Current Through Diode (I_1)**: The current through the diode depends on the voltage across it and the temperature. The expression for current through the diode is given by:
  \[ I_1 = f(T) \]
  where \( f(T) \) represents the temperature-dependent function.

- **Current Through Resistor (I_2)**: The current through the resistor is given by:
  \[ I_2 = \frac{V}{R} \]
  where \( V \) is the voltage across the resistor and \( R \) is the resistance.

**Diode Compensation**:

The compensation circuit is designed to ensure stability against temperature variations. The diode compensates for changes in the current source \( I_e \) due to temperature fluctuations. The compensated current \( I_e' \) is given by:

\[ I_e' = I_e + k(T - T_0) \]

where \( k \) is the temperature coefficient, and \( T_0 \) is a reference temperature.

**Operational Logic**:

The circuit operates by stabilizing the current source against temperature changes, ensuring consistent performance across different temperatures.
\[ T \uparrow \quad I_0 \uparrow \quad I_e \uparrow \]

\[ J_C = \beta J_B + (1 + \beta) J_{e0} \]

\[ J_B = I_B + I' \]

Simultaneously

\[ T \uparrow \quad R_s \uparrow \quad I_s \downarrow \]

\[ I_s = I_B + I' \]

... when \( I_s \) decreases, \( I_B \) also decreases.

\( I_{e0} \uparrow \) \( \text{and} \quad I_B \downarrow \) \( \text{so effect cancel out.} \)

* **Biasing Circuits**:  

(i) Fixed Biased Circuit  
(ii) Collector to base bias circuit  
(iii) Self Bias / Voltage divider bias / Potential divider bias

**Fixed Biased Circuit**:  

\[ S = 1 + \beta \]

\[ \text{Stability factor very high.} \]

So non practical circuit

\[ V_{cc} + J_B R_B + V_{BE} = 0 \]

\[ I_B = \frac{V_{cc} - V_{BE}}{R} \]

As the value of \( I_B \) is fixed so it called fixed bias circuit.
There is no provision to decrease $I_B$, so stability factor is high. So practically not used.

2) Collector to Base bias Circuit:

Applying input loop:

$$-Vcc + (I_B + I_c)R_c + I_B R_B + V_{BE} = 0$$

$$I_B (I_B + R_c) = Vcc - V_{BE} - I_c R_c$$

$$I_B = \frac{Vcc - V_{BE}}{I_B + R_c} - \frac{I_c R_c}{(R_B + R_C)_{fixed}}$$

When $T \uparrow$, $I_{co} \uparrow$ hence $I_c \uparrow$
giving

$$I_c = \beta I_B + (1 + \beta) I_{co}$$

$I_B$ is decreases by eqn 1
Hence effect cancel out.

$$S = \frac{1 + \beta}{1 + \beta R_C / R_{thc}}$$

$$I_c = \frac{1 + \beta}{1 + \beta R_C / R_{thc}}$$

$$V_{BE} = 0.9V$$

$$\beta = 100$$

$$S = 10$$

$$R_B = 9R_C$$
\[ I_0 = \frac{10}{(R_8 + 3) + 300} \]

\[ \log \left( \frac{R_8 + 3}{300} \right) = \log (R_8 + 3) \]

\[ 10R_8 + 30 + 300 \approx 10 \log R_8 + 30 \approx \]

\[ 10 \log R_8 - 10 \log R_B = -303 + 30 + 300 \approx \]

\[ R_B (\text{in}) = 27.27 \]

\[ \frac{27.27}{91} \approx 29.967 \]

\[ R_B \approx 30k \]

\[ -10 + (I_B + I_C) \times 3k + I_B \times 30k + 0.7 = 0 \]

\[ I_B \times 3.3k + I_C \times 9k = 9.3 \]

\[ I_B \times 3.3k = I_B \times 800k + 9.3 \]

\[ \{ I_C = \beta I_B \} \]

\[ I_B = \frac{9.3}{337k} = 0.02 \]

\[ I_C = 10 \times 0.02 \]

**Applying in outward loop:**

\[ -10 + I_E \times 3k + V_{CE} = 0 \]

\[ V_{CE} = 10 - I_E \times 3k \]

\[ V_{CE} = 3.44V \]
\[ S = \frac{1 + \beta}{1 + \frac{\beta R_c}{R_B + R_c}} \]

\[ S = \frac{1 + \beta (R_B + R_c)}{(R_B + R_c) + \beta R_c} \]

\[ \therefore \beta \text{ is very large} \]

So:

\[ S = \frac{\beta (R_B + R_c)}{\beta R_c} = \frac{R_B + R_c}{R_c} \]

\[ 10 = \frac{R_B + 3}{3} \]

\[ 30 = R_B + 3 \]

\[ R_B = 30 - 3 = 27 \]
Thévenin's Theorem:

For any linear and bilateral network seen from two terminal A, B the simplified representation a voltage source \( (V_{th}) \) and a single resistance \( (R_{th}) \) in series with \( (V_{th}) \).

\[
\frac{3d^2y}{du^2} + q \frac{dy}{du} + 3y + \Omega = 0.
\]

So given eqn is non-linear eqn.

Linear graph must passing through the origin.

Ohm's law:

\[ V = I \times R \]
Simplified diagram.

\[ V_{cc} = V_{in} \]

\[ R_1, R_2 = \text{from voltage divider rule.} \]

\[ V_{th} = \frac{V_{cc} \times R_1}{R_1 + R_2} \]

\[ A = \frac{1 + \beta}{1 - \beta \frac{R_E}{R_E + R_E}} \]
\[-V_{th} + I_B R_B + V_{BE} + I_E R_E = 0\]
\[-V_{th} + I_B R_B + V_{BE} + (I_E + I_E) R_E = 0\]
\[I_B (R_B + R_E) + I_E R_E = V_{th} - V_{BE}\]

\[I_B = \frac{V_{th} - V_{BE}}{R_B + R_E}\]
\[I_E R_E = \frac{I_E R_E}{R_B + R_E}\]

"As temp increases, \(I_{co}\) increases and \(I_c\) also increases given by -

\[I_c = \beta I_B + (\beta + 1) I_{co}\]

Simultaneously, \(I_B\) decreases given by eqn (1). Increase in \(I_{co}\) decreases in \(I_B\), thus the effect cancels out. Hence \(I_c\) will be stable.

<table>
<thead>
<tr>
<th>Bias</th>
<th>Stability Factor</th>
<th>Approximate Analysis (Stages)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed</td>
<td>(S = 1 + \beta)</td>
<td>(\beta)</td>
</tr>
</tbody>
</table>

- C-B Bias: \(-\frac{1}{R_E}\)
- C-A Bias: \(\frac{V_{BE}}{K_B}\)
- S-A Bias: \(1 + \frac{K_A}{K_B}\)
Q. For the given circuit diagram draw the load line, calculate Q-point, determine the stability factor.

\[ V_{EE} = 10V \]
\[ V_{BE} = 0.7V \]
\[ R_C = 31K \]
\[ R_E = 2K \]

\[ I_C = \frac{10}{5} = 2mA \]

\[ V_{CC} = 10V \]

\[ -5 + I_B \times 50 + 0.7 + I_E \times 2K = 0 \]

\[ \Rightarrow -5 + I_B \times 50 + 0.7 + (I_B + I_E) \times 2K = 0 \]

\[ \Rightarrow 52I_B + 250I_E = 9.3 \]

\[ \Rightarrow 52I_B + 250I_B = 9.3 \]

\[ I_B = 0.047mA \]

\[ I_E = \frac{9.3}{252K} = 0.017mA \]

\[ I_C = \beta I_B \]

\[ I_C = 100 \times 0.017 \Rightarrow I_C = 1.7mA \]
\[-10 + I_C \times 3 + V_{CE} + I_E \times R_E = 0\]
\[3I_C + V_{CE} + I_B R_E + I_C R_E = 10\]
\[5I_C + 0.017 \times 2 = 10 - V_{CE}\]
\[V_{CE} = \]

\[S = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_B + R_E}} = \frac{1 + 100}{1 + 100 \times \frac{50}{50 + 2}} = \frac{101}{1 + 100 \times \frac{50}{50 + 2}}
\]
\[S = \frac{101 \times 5^2}{5^2 + 100 \times 5^0}\]

\[10) \text{ for the given circuit diagram determine the resistances}\]

\[\beta = 100\]
\[Q \quad [\text{em.A}]/\text{V}\]
\[S = 10\]
\[V_{BE} = 0.7\]
\[ R_B = \frac{R_1 R_2}{R_1 + R_2} \]

\[ V_{th} = \frac{V_{cc} R_1}{R_1 + R_2} \]

\[ \frac{R_B}{V_{th}} = \frac{R_1 R_2}{V_{cc} R_1} = \frac{R_2}{V_{cc}} \]

\[ \frac{R_2}{V_{th}} = \frac{R_2}{V_{cc}} \]

\[ S = \frac{1 + \beta}{1 + \beta \cdot \frac{R_E}{R_B + R_E}} \Rightarrow \frac{10}{1 + \frac{100}{R_B + 1}} = 10 \]

\[ \frac{(101) (R_B + 1)}{R_B + 101} = 10 \]

\[ 10R_B + 1010 = 101R_B + 10 \]

\[ \Rightarrow 91R_B = 1010 - 101 \]

\[ 91R_B = 909 \]

\[ R_B = \frac{909}{91} \]

\[ \approx 9.9 \approx 10 \]

\[ R_B = 10k \]

\[ (2m \cdot A, 8V) \]

\[ I_C = 2m \cdot A, V_{CC} = 8V \]

\[ I_B = \frac{I_C}{\beta} = \frac{2}{100} = 0.02 \text{ m} \cdot A \]
\[ I_B = 0.02 \text{mA} \]

\[-V_{th} + I_B \times R_B + \frac{V_{BE}}{I_B} + I_C \times R_E = 0 \]

\[ I_E = \frac{V_{th} - V_{BE}}{I_B \times R_B} \]

\[ I_B + I_C = \frac{V_{th} - 0.7}{0.2 \times 10} \]

\[ V_{th} = \frac{0.2}{0.2} (2.02) + 0.7 \]

\[ V_{th} = 2.9 \text{V} \]

\[ \frac{R_B}{V_{th}} = \frac{R_O}{V_{CC}} \]

\[ R_O = \frac{V_{CC} \times R_B}{V_{th}} = \frac{16 \times 16}{2.9} \]

\[ R_O = \frac{160}{2.9} \text{K} \]

\[ R_B = \frac{R_1 \times R_O}{R_1 + R_O} \]

Applying Johnson:

\[-16 + I_C \times R_C + V_{CE} + I_C \times R_E = 0 \]

\[ R_C = \frac{2 \times 0.02 + 16 - 8}{2} = \frac{-2 \times 0.02 + 8}{2} \]

\[ = \frac{5.98}{2} = 2.98 \text{V} \]

\[ R_C = 2.98 \approx 3 \text{V} \]
\[ I_C = I_E = \beta I_B \]

\[ I_B = 1.2 \text{ mA} \]

\[ I_E = I_C = 1.2 \text{ mA} \]

\[ I_B = 1 \text{ mA} \]

\[ I_E = 1 \text{ mA} \]

\[ I_C = 1 \text{ mA} \]

\[ I_C = 1.2 \text{ mA} \]

\[ V_{th} = \frac{V_{cc} \times R_1}{R_1 + R_2} \]

\[ R_B = \frac{R_1 R_2}{R_1 + R_2} \]

\[ R_B = 9 \text{ k}\Omega \]

\[ q = \frac{R_B}{I} \]

\[ S = 1 + \frac{R_B}{R_E} \]

\[ 10 = 1 + \frac{R_B}{R_E} \]

\[ v_{th} = \frac{V_{cc} \times R_1}{R_1 + R_2} \]

\[ \frac{R_B}{v_{th}} = \frac{R_2}{V_{cc}} \]
\[ R_{e} = \frac{R_{1}R_{2}}{R_{1} + R_{2}} \]

\[ q = \frac{R_{1} \times 58.33}{R_{1} + 58.33} \]

\[ 9R_{1} + 9 \times 58.33 = R_{1} \times 58.33 \]

\[ 9 \times 58.33 = R_{1} \times 58.33 - 9R_{1} \]

\[ R_{1} = \frac{9 \times 58.33}{(58.33 - 9)} \]

\[ R_{1} = 10.8272 \]

\[ V_{cc} \geq \frac{12}{R_{c}} \geq 6 \text{ mA} \]

\[ V_{CE} \leq 0.3 \]

\[ R_{C} = 9k \]

\[ V_{BE} = 0.3 \]

\[ 12V \]

\[ V_{cc} = 12 \text{ V} \]

\[ R_{c} = \frac{V_{cc}}{I_{C}} \geq 6 \text{ mA} \]

\[ I_{C} = 0.03 \text{ mA} \]

\[ V_{ce} = 30 \text{ V} \]
\(-15V + I_B \times 100K + 0.7 + (I_B + I_C) \times 1\mu\Omega = 0 \)

\(I_B \times 100K + (I_B + I_C) 0.1K = 19.3 \)

\(I_B \times 100K + (I_B + 100I_B) \times 0.1K = 19.3 \)

\(I_B \left( 100K + 10.1K \right) = 19.3 \)

\[ I_B = \frac{19.3}{110.1} \text{ mA} \]

\[ I_B = 0.17 \text{ mA} \]

\(I_C = \beta I_B\)

\(I_C = 100 \times 0.13 \text{ mA} \)

\[ I_C = 13 \text{ mA} \]

\(-15 + I_C \times 0.9 + V_{CC} + (I_B + I_C) 0.1K = 0 \)
-5V + \frac{I_B}{1k} + 0.7 = 0

\Rightarrow I_B = 9.3 \text{ m.A.}

\beta = \frac{I_C}{I_B}

I_C = 9.3 \times 10^{-3} \times 10^{3} A

I_C = 0.093 A

\frac{R_g - 1.3}{0.677} \text{ Ans (c)}
* Power Dissipation in the Transistor:

Power dissipation in emitter junction:
\[ P_E = V_{BE} \times I_E \quad \cdots (1) \]

Power dissipation in collector junction:
\[ P_C = V_{CB} \times I_C \quad \cdots (II) \]

Total Power
\[ P_T = P_E + P_C \]
\[ = V_{BE} \times I_E + V_{CB} \times I_C \]
\[ \frac{P_T}{I} = V_{CE} I_C + V_{RE} I_C \]
\[ I_t = (V_{EB} + V_{BE}) I_C \]
\[ I_t = V_{CE} I_C \]

\[ -2 + 0.7 + I_C \times 100 = 10 \]
\[ I_C = \frac{1.3}{100} \]
\[ I_C = 13 \text{ mA} \]

\[ -15 + 13 \times 0.5 + V_{CE} + 13 \times 0.1 = 0 \]
\[ V_{CE} = 8.15 + 6.5 + 1.3 \]
\[ = 15 - 7.8 = 7.2 \]
\[ V_{CE} = 7.2 \text{ V} \]

\[ P = V_{CE} \times I_C \]
\[ = 13 \times 7.2 \]
\[ P = 93.6 \text{ mW} \text{答} \]

**Second Method:**

\[ -V_{CE} \]
2. For the given circuit diagram calculate power dissipation across the transistor.

From previous graphs:

\[ I_C = 1.5 \text{ mA} \]
\[ V_{CE} = 1.9 \text{ V} \]
\[ I_B = 0.017 \text{ mA} \]

\[ P_I = (1.7 \times 1.4) \text{ mW} \]
\[ P_I = 2.4 \text{ mW} \]

Exact Method:

\[ V_{CB} = V_{CE} - V_{BE} \]
\[ = 1.96 - 0.7 \]
\[ \boxed{V_{CB} = 0.76 \text{ V}} \]

\[ P_I = V_{BE} \times I_E + V_{CB} \times I_C \]
\[ = 0.7 \times 1.751 + 0.76 \times 1.7 \]
\[ = 1.2011 + 1.292 \]
\[ \boxed{P_I = 2.49 \text{ mW}} \]

2. For the given circuit diagram find power dissipation.
Field Effect Transistor

The device operating under the influence of electric field. It is a unipolar device i.e. single type of charge carriers involved in the conduction process only majority carriers present & minority carriers negligible hence minority carrier current also negligible, hence device is independent of temp. Hence thermally stable.

* Construction of Junction Field Effect Transistor

Field Effect Transistor

\[ \text{JFET} \]

8-terminal device

\[ \rightarrow \text{Source} \rightarrow \text{Emitter} \]

\[ \rightarrow \text{Drain} \rightarrow \text{Collector} \]

\[ \rightarrow \text{Gate} \rightarrow \text{Base} \]

\[ \text{n-channel} \quad \text{p-channel} \]

\[ \Rightarrow \text{MOSFET in having very high input resistance as compared to JFET because Oxide layer is used in MOSFET. } (S_2 + O_2 \rightarrow \text{MOS}) \]
* Construction of n-channel JFET:*

FET is a "symmetrical" device because drain and source are interchangeable but BJT is a non-symmetrical device because collector & emitter are not interchangeable.

* Biasing of JFET:*

(Biasing means how to apply the voltage to work the device.)
for the analysis of the transistor since gate is reverse biased then \( I_G = 0 \).

* Transfer Characteristic *

Since input current \( I_G = 0 \), it is not possible to draw input characteristic. Hence transfer characteristics are implemented.

The shape of the depletion region is larger near gate, drain, and source. The shape of depletion layer is wedge shape.
When \( V_{gs} = 0 \) the current through the channel is maximum. As \( V_{gs} \) increases reverse bias voltage increases.

The depletion region will move towards each other, the flow of charge carriers reduces. Hence current also decreases.

As \( V_{gs} \) increases to such an extent the two depletion region penetrate in each other current through the channel is zero that voltage is called pinch-off voltage (\( V_{gs} \) cut off or \( V_{gs} \) off).

\[
I_D = I_{DSS} \left( 1 - \frac{V_{gs}}{V_p} \right)^2
\]

\[\rightarrow \text{ It is a square law device.}\]

\* Transconductance:

\[
\frac{\partial I_D}{\partial V_{gs}} = \frac{\partial}{\partial V_{gs}} \left[ I_{DSS} \left( 1 - \frac{V_{gs}}{V_p} \right)^2 \right]
\]

\[= I_{DSS} \frac{\partial}{\partial V_{gs}} \left[ 1 - \frac{V_{gs}}{V_p} \right]^2
\]

\[= 2 I_{DSS} \left[ 1 - \frac{V_{gs}}{V_p} \right] \left[ -\frac{1}{V_p} \right]
\]
\[ g_m = - \frac{2}{V_p} \left[ 1 - \frac{V_{gs}}{V_p} \right] \]

* Maximum Transconductance:

\[ (g_m)_{\text{max}} = - \frac{2 I_{DSS}}{V_p} \quad (\therefore V_{gs} = 0) \]

Q. An n-channel junction field effect transistor law:

\[ I_{DSS} = 10 \text{mA}, \quad V_{gs} = -2 \text{V}, \quad V_p = -8 \text{V} \]

Calculate \( I_D \), \( g_m \), \( (g_m)_{\text{max}} \).

\[ I_D = 10 \left[ 1 - \frac{8}{8} \right]^2 \]

\[ = 10 \left[ \frac{0}{84} \right] \]

\[ I_D = 5.6 \text{mA} \]

\[ g_m = \frac{+2 \times 10^{-3}}{V_p} \left[ 1 - \frac{8}{8} \right] \]

\[ = \frac{5}{2} \left( \frac{6-3}{6} \right) = \frac{1.5}{6} \]

\[ g_m = 1.8 \frac{\text{mS}}{\text{V}} \text{ or } V \cos \theta \]
\[
(q_m)_{\text{max}} = \frac{-12 \times 10}{78.4}
\]

\[
(q_m)_{\text{max}} = 2.5 \text{ times.}
\]

For the given circuit diagram:

\[
I_{DSS} = 10 \text{ mA.}
\]

\[
V_P = -10 \text{ V}
\]

\[
I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 + 2 + I_g \times 98k + V_{GS} = 0
\]

\[
\Rightarrow I_g = 0
\]

\[
\Rightarrow V_{GS} = -2 \text{ V}
\]

\[
I_D = 10 \left[ 1 - \frac{2}{10} \right]^2 = 10 \times \frac{8}{10} \times \frac{8}{10}
\]

\[
I_D = 0.64 \text{ mA}
\]
\[(g_m)_{\text{max}} = \frac{12 \times 10^3}{\sqrt{16}} = 2\]

\[(g_m)_{\text{max}} = 2\]

\[g_m = -\frac{2 J q_s}{V_p} \left(1 - \frac{V_{gs}}{V_p}\right)\]

\[= \frac{2 \times 16 \text{ mV}}{16} \left[1 + \frac{2}{10^5}\right]\]

\[= 2 \times \frac{4}{5} = \frac{8}{5}\]

\[g_m = 1.6\]

\[Q_{88}\]

\[\text{Check - } 3.16\]

\[I_{DSS} = 5 \text{ mA}\]

\[V_p = -5\]

\[V_{gs} = -2.5\]

\[I_D = I_{DSS} \left[1 - \frac{V_{gs}}{V_p}\right]^2\]

\[= 5 \left[1 - \frac{2.5}{-5}\right]^2\]

\[= 5 \times 16\]

\[= 80\]
Always $I_S = I_D$ (for numerical value)

$$I_D = \frac{20 - 10}{2} = \frac{10}{2} = 5 \text{ mA}.$$ 

Q. An n-channel JFET having $I_D$ changes from 3 mA to 8.1 mA if $V_{gs}$ changes from (-2 to -1.8) Volt. Find transconductance $g_m$.

$$g_m = \frac{dI_D}{dV_{gs}} = \frac{(3.1 - 3)}{(-1.8 - (-2))} = \frac{0.1}{0.2} = 0.5 \frac{\text{mA}}{V}$$

Q. For the given circuit diagram find $I_D$, $I_S$, $V_0$ shown in figure.
\[ V_g = \frac{20 \times 90}{20 + 90} = \frac{400}{100} = 4 \text{ V} \]

\[ V_g = 4 \text{ V} \]

\[-q + J_s \times 16k + V_{gs} + J_s \times 2k = 0\]

\[-q + (-2) + J_s \times 2k = 0\]

\[ J_s = \frac{6}{2} = 3 \text{ mA} \]

In second loop:

\[-20 + I_d \times 3 + V_o = 0\]

\[ V_o = 20 - I_d \times 3\]

\[ V_o = 20 - 3 \times 3\]

\[ V_o = 11 \text{ V} \]
Determine the voltage $V_{DS} = \gamma$

$-20 + ID \times 3k + V_{DS} + IS \times 2k = 0$

$-20 + 3mA \times 3k + V_{DS} + 3mA \times 2k = 0$

$V_{DS} = 20 - 9 - 6$

$V_{DS} = 5V$

Second method:

$V_0 = +V_{DS} + IS \times 2k$

So $V_{DS} = V_0 - IS \times 2k$

$= 11 - 3 \times 2$

$= 11 - 6$

$V_{DS} = 5V$

* Source Transformation: always

In parallel, by always $R$

$$V = \frac{V}{R}$$

In series, by always $R$

$$V = IR$$

In parallel, by always $R$
\[ R_{11} = \frac{R_1 R_2}{R_1 + R_2} = \frac{12 \times 6}{12 + 6} = \frac{18 \times 6}{18} = 9 \text{kΩ} \]
Q. For the given circuit diagram

\[ \frac{16}{1} + \frac{1}{(8+2)} \frac{1}{8} + 0.6 = 0 \]

\[ \log I = 15.9 \]

\[ I = \frac{15.9}{10} \]

\[ I = 1.59 \text{ mA} \]

Q. Convert the entire circuit into single current and single resistance.
\[ R_{11} = \frac{4 \times 9 \times 4}{9 + 2 + 4} = \frac{9 \times 2}{9 + 2} = \frac{8}{6} = \frac{8}{3} \times 4 = \frac{16}{3} \times 4 = 1 \text{ k} \]

\[ R_{11} = 1 \text{ k} \]

\[ 2 \text{ m} \Omega \]

*Output characteristics of JFET*
When $V_{DS}$ applied the two depletion region will try to move towards each other simultaneously a potential difference is applied hence electric field generated in the channel pointing from $+V_s$ to $-V_s$ (Drain to Source) which will maintains a constant gap between two depletion region, hence constant amount of current flows through the channel.
* Analog to Digital Converter And Digital to Analog Converter

* Analog to Digital Converter:
* Counter type ADC <-> Basic Converter
* Successive approx type ADC <-> Uniform Converter
* Flash type Converter ADC <-> Fastest Converter or Simultaneous Converter
* Dual slope Converter ADC <-> Slowest Converter

* Digital to Analog Converter:
* Weighted register type
* R to 2R ladder network

* Characteristic Properties of Digital to analog Converter:
  → Different parameters of Converter:
  1. Resolution
  2. Percentage Resolution
  3. Full scale Voltage
  4. Analog Voltage
1. Resolution:

Due to increment at 1-bit in L.S.B., change in the analog voltage the change is called as resolution.

\[ \text{Resolution} = \frac{V_r}{2^n-1}. \]

\( V_r \) = Voltage applied to corresponding to logic 1.

2. Percentage Resolution:

\[ \frac{V_r}{2^n-1} \times 100\% \]

\( n = \) no. of bits

\[ \text{Y. Resolution} = \frac{1}{2^n-1} \times 100\% \]

3. Full Scale Voltage:

\[ V_{fs} = V_r \quad (\text{always}) \]
Analog Voltage:

\[
\text{Analog voltage} = \text{Resolution} \times \text{Decimal equivalent}
\]

Ex -

\[
\begin{array}{cccc}
5.2 & 101 \\
6.2 & 110 \\
7.2 & 111 \\
\end{array}
\]

\[
x + 7 = 111
\]

It is agility to Analog converters having \( X = 0.4 \).

Identify number of bits involved in the conversion.

Soln -

\[
\text{Res} = 0.4 \times 100 = \frac{1}{2^{n-1}} \times 100 \\
\]

\[
\Rightarrow \frac{0.4}{100} = \frac{1}{2^{n-1}}
\]

\[
\Rightarrow 1000 = 2^{n-1}
\]

\[
\Rightarrow 2^{n-1} = 256
\]

\[
\Rightarrow 2^n = 256
\]

\[
\Rightarrow 2^n \approx 2^8
\]

\[
\therefore n = 8
\]

So, the number of bits not in the fraction or decimal is

\[
\text{We write } 2^7 \cdot 9 \Rightarrow 28 \text{ in place of } 251 \text{ we write } 25
\]
A 8-bit digital-to-analog converter having voltage applied corresponding to logic 1 = 10V. Calculate

1. \( R = \frac{V_{fs}}{2^{n-1}} = \frac{10}{2^{7-1}} = \frac{10}{63.5} = 0.16 \)

2. \( V_{fs} = 10V \)  \( \therefore \) \( V_{fs} = 10V \)

\( 0.93 \times 10 = 9.3 \)

\( V = 0.42 \)
A 3-bit digital to analog to digital converter has an applied voltage ranging from -10 V to +10 V. Calculate resolution and % resolution.

So

\[ R = \frac{V_r}{2^n-1} \]

\[ V_r = \text{potential difference} \]

\[ V_r = 10 - (-10) = 20 \text{ V} \]

So

\[ R = \frac{20}{2^3-1} = \frac{20}{7} \]

\[ R = 2.86 \text{ V} \]

% R = \frac{1}{2^n-1} \times 100 \%

\[ = \frac{1}{7} \times 100 \%

\[ R = 14.28 \text{ %} \]
\[ R = \frac{1}{2^{6n-1}} = \frac{1}{63-1} = \frac{1}{62} \]

\[ R = 0.01587 \]

\[ A = R \times 20 \]

\[ A = 0.3174 \]

\[ V_r = 10 \]

\[ R = \frac{10}{2^{6r-1}} = \frac{10}{63} = 3.17 \]

\[ A = \frac{10}{63} \times 20 = \frac{200}{63} \]

\[ A = 63.49 \]

---

88 The high input impedance of field effect transistor (FET) amplifier is due to:

a) The pinch-off voltage  

b) The very slow gate current

c) The source and drain being far apart  

d) The geometry of the FET
Modulation

\[ f(x) \xrightarrow{\text{it}} f(x) \]

\[ f(x) \xrightarrow{G_x w_o x} \frac{1}{2k} \left[ f(x-w_o) + f(x+w_o) \right] \]

\[ \text{Power} = \frac{\text{Energy}}{\text{Time}} \]

\[ \text{Power} = \text{Energy} \times \text{Frequency} \]

* Modulation is used to increase the strength of a signal so that it can travel a large distance into the space (wireless communication).

\[ X = 7 \text{ MHz} \]

or 
\[ w_0 = 10 \text{ KHz} \]

\[ w_0 = 0.01 \text{ MHz} \]

\[ S_0 = X-w_0 \rightarrow X+w_0 \]

\[ = 7-0.01 \rightarrow 7+0.01 \]

\[ = 6.99 \rightarrow 7.01 \text{ MHz} \]
Analog to Digital Converter

* Counter type Converter:

![Diagram of a counter type converter]

When all the difference of comparator is +ve, output assumed as 1. Clock will enter into the counter, count sequence increases.

When the difference of op-amp becomes -ve output becomes zero. Clock will stop entering into the counter. The binary value at which count stop will be considered as digital output for the applied analog output.

* When applied voltage is 1V (~0.9V) then minimum clock pulse required is one.
  maximum number of clock pulse required = \(2^{n-1}\).

Minimum conversion time = \(1 \times T\) clock

Maximum = \((2^{n-1}) \times T\) clock.

(Memorize)
Successive Approximation type Converter:

Whenever difference of op-amp either +ve or negative register will perform Shift operation but control circuit is designed in such a way that when difference is 1 during shifting the previous bit which was 0 during shifting operation will be kept as it is, when previous bit which was set (1) becomes zero (-ve).

S.A.R. type converter is independent of applied voltage only depends on number of bits.

No. of Clock pulse required = n

V_0 > V_r = 1100
V_0 < V_r = 0100
V_r < V_r = 0011
Maximum conversion time = n x T clk

* Flash Type Converter *

Number of used registers = 2^n
n = no. of bits
No. of k registers = 2 (for 2-bit)
No. of comparators (Op-amp) = (2^n - 1)

<table>
<thead>
<tr>
<th>( i / p )</th>
<th>( y_1 )</th>
<th>( y_0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_a &lt; V_x/4 )</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( V_x/4 &lt; V_a &lt; V_x/2 )</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( V_x/2 &lt; V_a &lt; 3V_x/4 )</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>( V_a &gt; 3V_x/4 )</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
A 12-bit converter (ADC), time period of one clock pulse 12 μSec. Its maximum conversion time is 14 μSec. Then the type of converter may be:

(a) Counter type
(b) SAR type
(c) Flash type [x]
(d) Dual Slope type.

Solve:

\[ T_{\text{clk}} = 12 \, \mu\text{s} \]
\[ n = 12 \]
\[ \text{max}^m \text{ Conv} = 14 \, \mu\text{sec} \]

\[ 1 \times 12 = 12 \, \mu\text{sec} \times 14 \, \mu\text{sec} \]
* Digital to Analog Converter:

1. Weighted Register Type
2. R-2R Ladder Type

\[ V_{MSB} \]  

The branch which is having minimum current represent L.S.B., for maximum branch current represents M.S.B.

Value of maximum resistance = \( 2^{(n-1)} \)

Q. For the given op-amp network shown if the minimum value of resistance is 1 kΩ. Identify current flowing through:

1. M.S.B.
2. L.S.B.
3. O/P Voltage.

Identify the binary value corresponding to which O/P is calculated.
\[ I_{MSB} = \frac{5-0}{1k} = 5 \text{ mA}. \]

\[ I_{MSB} = 5 \text{ mA}. \]

\[ I_{LSB} = \frac{5-0}{0} = \infty = 0.625 \text{ mA}. \]

\[ I_{LSB} = 0.625 \text{ mA}. \]

\[ I_1 + I_2 + I_3 + I_4 + I_5 = 0 \]

\[ 5 \text{ mA} + 0.625 \text{ mA} + \frac{V_0 - 6}{10k} = 0 \]

\[ \frac{V_0}{10} = -5.625 \text{ mA}. \]

\[ V_0 = -56.25 \text{ V} \]

\[ M_{SB} \]

\[ L_{SB} \]

\[ \begin{pmatrix} 1 & 0 & 0 & 1 \end{pmatrix} \]

\[ (5V) \]

\[ = 9 \]
Q. R-2R Laddler Network:

\[
\text{Decimal voltage} = \frac{V}{2^n-1} \times \text{decimal equi.}
\]

Q. For the given circuit diagram calculate the analog OP-0 voltage shown in figure.
\[ V = \frac{10}{8^{3+1}} \times 5^- = \frac{50}{7} = 7.1V. \]

\[ \frac{V_0}{7.1} = -\frac{R_6}{R_1} \]

\[ \frac{V_0}{7.1} = -\frac{10k}{1k} \]

\[ V_0 = -71V \]

Q: For the given network calculate analog output voltage.

\[ \frac{V_x}{8^{n-1}} \times \text{decimal equivalent.} \]

\[ V = \frac{10}{8^{9+1}} \times 13 = \frac{10}{15} \times 13 = \frac{150}{18} = 8.6V. \]

\[ V = 8.6V \]
\[
\frac{8.6 - V_{a1}}{1K} = 0 \times 0
\]

\[V_{a1} = 8.6 \text{ V} \]

\[\sum_i + \sum_i = 0\]

\[
\frac{0 - 8.6}{1K} + \frac{V_0 - 8.6}{10K} = 0
\]

\[
\frac{V_0 - 8.6}{10K} = 8.6
\]

\[V_0 - 8.6 = 0\]

\[V_0 = 8.6 + 8.6 \]

\[V_0 = 17.2 \text{ V} \text{ (Ans)}\]

\[
\frac{V_0 - 8.6}{K} = 0
\]

\[V_0 = 8.6 \text{ V} \]
\[ Z_i = \infty \]

\[ v_i = f(I_i, V_i) = \infty \]
\[ i_o = f(I_i, V_o) = 0 \]

Now \[ v_1 = h_1 I_1 + h_2 V_2 \]
\[ I_2 = h_3 I_1 + h_4 V_2 \]

\[ \Rightarrow -v_1 + h_1 I_1 + h_2 V_2 = 0 \]

So, draw circuit:

\[ V_1 = h_1 I_1 + h_2 V_2 \]
\[ I_2 = h_3 I_1 + h_4 V_2 \]

When 0 \text{ Volts} \Rightarrow 0 \text{ means} \[ V_2 = 0 \]

then, \[ h_1 = \frac{V_1}{I_1} = h_i \]

\[ h_3 = \frac{I_2}{I_1} \text{ means it is gain (constant) } = h_f \]
\[ I_1 = 0 \]

\[ V_1 = h_2 V_2 \]

\[ h_2 = \frac{V_1}{V_2} = h_r = \text{Reverse voltage gain.} \]

\[ \Rightarrow I_2 = h_4 V_2 \]

\[ h_4 = \frac{I_2}{V_2} = h_0 = \]

\[ \begin{array}{c}
  + \quad h_i \quad \rightarrow \quad I_1 \\
  \downarrow \quad \hline \\
  \hat{I}_1 \quad + \quad h_r \quad I_1 \\
  \downarrow \quad \hline \\
  V_1 \\
  - \\
  \uparrow \quad h_o \quad V_2 \\
  + \\
  \downarrow \quad \hline \\
  I_2 \\
  - \end{array} \]

<table>
<thead>
<tr>
<th></th>
<th>CE</th>
<th>C.C</th>
<th>CB</th>
</tr>
</thead>
<tbody>
<tr>
<td>( h_i )</td>
<td>( h_{ie} )</td>
<td>( h_{ic} )</td>
<td>( h_{ib} )</td>
</tr>
<tr>
<td>( h_r )</td>
<td>( h_{re} )</td>
<td>( h_{rc} )</td>
<td>( h_{rb} )</td>
</tr>
<tr>
<td>( h_4 )</td>
<td>( h_{fe} )</td>
<td>( h_{fc} )</td>
<td>( h_{fb} )</td>
</tr>
<tr>
<td>( h_0 )</td>
<td>( h_{oe} )</td>
<td>( h_{oc} )</td>
<td>( h_{ob} )</td>
</tr>
</tbody>
</table>

For a FET, \( A_i \), \( R_{in} \), \( R_{out} \) \( \Rightarrow \) when we can not apply loop we can apply above steps.
Current Gain:

\[ A_I = \frac{\text{Current gain}}{I_L = -I_2} \]

\[ V_2 = I_L R_L \]

\[ V_2 = -I_2 R_L \]

\[ I_2 = h_f I_1 + I_2 \]

\[ I_2 = h_f I_1 + V_2 h_0 \]

\[ I_2 = h_f I_1 - I_2 \cdot R_c h_0 \]

\[ I_2 + I_2 h_0 R_i = h_f I_1 \]

\[ I_2 \left[ 1 + h_0 R_i \right] = h_f I_1 \]

\[ \frac{I_2}{I_1} = \frac{h_f}{1 + h_0 R_i} \]

Input Resistance:

\[-V_1 + I_2 h_i + h_{r_2} V_2 = 0 \]

\[ V_1 = h_1 I_1 + h_{r_2} V_2 \]

Now divided by \( I_1 \):

\[ \frac{V_1}{I_1} = h_1 + h_{r_2} \frac{V_2}{I_1} \]

\[ \frac{V_1}{I_1} = h_i + h_{r_2} \left( \frac{I_2}{I_1} \right) R_L \]
\[ Rin = \frac{V_1}{I_1} = h_i + h_r A_I R_L \]

* Voltage Gain \((A_V)\) -
\[ v = IR \]
\[ A_V = A_I R_g \]
\[ \text{So} \]
\[ A_V = A_I + \frac{R_L}{R_{in}} \]

* Output Resistance -
\[ R_o = \frac{1}{h_o} \]

Equivalent diagram -
\[ A_I = -\frac{h_f}{1+h} = -h_f \]
\[ R_{in} = h_i \]
\[ A_V = A_I R_L = \frac{A_I \cdot R_L}{R_{in}} \]
\[ R_o = \frac{1}{h_o} \]
Steps of A.C. Analysis:

1. Ground all the DC sources
2. Short all the capacitors
3. Draw the equivalent diagram for the calculation of equivalent load resistance and use that R_L in circuit analysis.

Q: for the given circuit get diagram calculate:
- Current gain, Voltage gain, input resistance and output resistance.

h_{ie} = 2.1K
h_{fe} = 100
h_{re} = 2 \times 10^{-4}
\beta_{0e} = 2 \times 10^{-6}

V_{cc} = 10V

\text{Solution: Equivalent diagram:}
\( A_I = -h_{fe} = -100 \)

\( R_i = 2K = h_i e \)

\( A_V = A_I \frac{R_L}{R_i} \)

\( A_V = -100 \times \frac{1.5K}{9K} = -7.5 \)

\( R_0 = \frac{1}{h_{oe}} = \frac{1}{2 \times 10^{-6}} = \)

Now from equations:

\( R_i = h_i e + h_{re} \times A_I \times K \)

\( = 2K + (9 \times 10^{-9}) \times (-100) \times 1.5 \)

\( R_i = 2 - \)
Q. For the given circuit diagram determine input resistance, output resistance, current gain, voltage gain.

\begin{align*}
&h_{ie} = 1.5 \text{k} \\
&h_{fe} = 200 \\
&h_{re} = 2 \times 10^{-5} \\
&h_{o}e = 2 \times 10^{-6} \\

&h_{ie} = 1.5 - h_{fe} = -200 \\
&h_{re} = 1.5 - h_{o}e = 1.5 - 2 \times 10^{-5} \\

&A_V = A_I \frac{R_o}{R_{in}} = -900 \times \frac{3 \times 10^{-5}}{1.5} = -900 \\

&R_o = \frac{1}{9 \times 10^{-6}} = 0.5 \Omega
\end{align*}
\[ A_I = -35 = -\frac{1}{h_{fe}} \]

\[ A_V = A_I \cdot \frac{R_L}{R_{in}} = -35 \times \frac{1000}{10000} \]

\[ A_V = -35 \]

2. For the given circuit diagram, calculate current gain, voltage gain, input resistance, and output resistance.
Equivalent circuit diagrams:

\[ A_I = -h_{fe} \]
\[ A_I = -100 \]
\[ R_{in} = h_{ie} = 2k \]

\[ A_V = A_I \frac{R_L}{R_{in}} \]
\[ = -150 \times \frac{2}{2} \]
\[ A_V = -150 \]

\[ R_0 = \frac{1}{h_{oe}} = \infty \]
Effect of RE in the circuit:

\[ V_i - V_{BE} = 0 \]

\[ V_i = V_{BE} \]

\[ -V_i + V_{BE} + I_E R_E = 0 \]

\[ V_{BE} = V_i - I_E R_E \]

Negative feedback.

- The presence of emitter resistor creates negative feedback.
- The presence of emitter resistor in circuit reduces the overall voltage gain because it decreases the capability of transistor to reach cut-in voltage.
RC-Coupled Amplifier:

When the output of (op-amp) any amp. directly connected with resistance (load) then it is called Direct coupled amplifiers.

When the output of any amp. connected with load via capacitor then it is called RC-Coupled amplifier.

In direct coupled amplifier output may contain d.c. and a.c. But in RC coupled amplifier output contains only a.c. becoz capacitor blocks d.c. hence called as blocking capacitor:

\[ X_c = \frac{1}{\omega C} \]

for d.c. \( T \to \infty, f = 0 \)

for d.c. \( T \to 0, f = \infty \)
\[-V_1 + I_1 h_{ie} + \left(h_{o e} V_2\right) + I_E R_E = 0\]

\[\Rightarrow h_{re} \approx \text{very large} \approx 0\]

\[\Rightarrow h_{re} V_2 \approx 0\]

\[V_1 = h_{ie} I_1 + \left(I_B + I_C\right) R_E\]

\[V_1 = h_{ie} I_B + \left(I_{B2} + I_C\right) R_E\]

\[V_1 = I_B h_{ie} + \left(I_B + \beta I_B\right) R_E\]

\[V_1 = I_B \left[h_{ie} + (1 + \beta) R_E\right]\]
\[
\frac{V_i}{I_{R_0}} = h_{ie} + (1 + \beta) R_e
\]

\[
R_{in} = h_{ie} + (1 + \beta) R_e
\]

\[A_V = \frac{h_{i3}}{h_{i3} + R_L \over R_{in}} \quad \text{so} \quad A_V \downarrow\]

<table>
<thead>
<tr>
<th>With CE</th>
<th>Without CE</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{in} = h_{ie} + (1 + \beta) R_e)</td>
<td>(h_{ie} + (1 + \beta) R_e = R_{in})</td>
</tr>
</tbody>
</table>

Q. For the given circuit diagram calculate \(A_V, A_I, R_{in}, R_0\)

\(h_{ie} = 2k\)
\(\beta = \frac{I_{CC}}{I_{C}} = h_{fe}\)
\(h_{o.c.} = 0\)
\(h_{re} = 0\)

\[
\frac{I_{in}}{I_i} = h_{fe} = \frac{I_{out}}{I_{R_0}} = \beta
\]

\[
\beta = \frac{I_{out}}{I_{R_0}}
\]
$A_I = -hfe = -100$

$R_{in} = hfe + Re(1+\beta) = 21\Omega + 2k(100+1) = 204\Omega$

$A_V = A_I \times \frac{R_L}{R_{in}}$

$= -100 \times \frac{2\Omega}{204}$

$A_V = \frac{\text{For the given circuit diagram determine approximate}}{\text{voltage gain.}}$

\[ \boxed{\begin{align*}
\text{a) } & -\frac{R_c}{R_E} \\
\text{b) } & \frac{R_c R_E}{R_E} \\
\text{c) } & \frac{R_c}{2} \\
\text{d) } & \frac{(R_c R_E)}{2}
\end{align*}} \]
\[ AV = n \frac{R_L}{R_{in}} \]

\[ AV = -\beta \frac{R_C}{R_E (1+\beta) + h_{ie}} \]

\[ R_{in} = R_E (1+\beta) + h_{ie} \]

\[ R_C = -\beta = -h_{fe} \]

\[ R_L = R_C \]

\[ \beta >> \gamma \]

\[ AV = -\beta \frac{R_C}{h_{ie} R_E} = -\frac{\beta R_C}{R_E} = -\frac{R_C}{R_E} \]

Q. For the given circuit diagram calculate the impedances overall input and output resistance and overall output resistance.

\[ h_{ie} = 2 \]

\[ h_{fe} = 100 \]

\[ h_{re} = 2 \times 10^{-6} \]
Equivalent

\[ A_f = -h_{fe} = -100 \]

\[ R_{in} = h_{re} = 2k \]

\[ A_v = \alpha J \frac{R_L}{R_{in}} = \frac{-100 \times \frac{2}{2}}{-150k} = -150k \]

\[ R_L = 0.5m\Omega \]

overall input resistance

\[ = \frac{80 \times 2.6}{80 + 190} = \frac{16 \times 2.6}{16 + 2} = \frac{32}{18} = 1.7 \times 500 \Omega \]

\[ = 0.5 + 1.7 = 2.2k\Omega \]
Overall output resistance -

\[ \frac{0.5 \times 3}{0.5 + 3} = \frac{1.5}{3.5} = 0.42 \text{ k}\Omega \]

\[ = 0.42 \text{ k}\Omega. \]

For the previous circuit calculate when:

- \( h_{ie} = 1 \text{ k}\)
- \( h_{fe} = 150 \)
- \( h_{re} = 0 \)
- \( h_{re} = 0 \)

A \[ A_S = -150 \]

\[ R_{in} = 1 \text{ k}\]

\[ A_{\mu} = -150 \times 3 \]

\[ \frac{1}{A_{\mu}} = -\frac{150}{3} \]

\[ R_0 = \frac{1}{h_{o}} = \infty \]
\[
\frac{80 \times 10}{20 + 10} = \frac{16 \Phi}{10\Phi} \quad \Rightarrow \quad \frac{16 \times 1}{16 + 1} = \frac{16}{17}
\]

\[
= \frac{16}{17} + 0.5 = \frac{16 + 8.5}{17}
\]

Overall \( \rac{1}{R} \) resistor = \frac{24.5}{17}

Overall \( \frac{1}{R} \) resistance = \( 3 \times \)
$C_1$ = Blocking as well as Coupling Capacitor
$C_2$ = Blocking Capacitor & Coupling Capacitor
$C_G$ = Bypass Capacitor
$R_1$ & $R_2$ = Biasing Resistor
$R_C$ is used for the calculation of $V_o$
Logic Families

These are the technologies which are used to implement the logic function.

Logic Families

- Saturated
  - Those logic families in which the devices enter into saturation region.
    - RTL (Resistor Transistor Logic)
    - DCTL (Direct Coupled Transistor Logic)
    - I2L (Integrated Injected Logic)
    - DTL (Diode Transistor Logic)
    - HSTL (High threshold transistor Logic)
    - TTL (Transistor-Transistor Logic)

- Non-Saturated
  - Device does not enter in the saturation region.
    - ECL [Emitter Coupled Logic]
    - CMOS [Complementary metal oxide semiconductor technology]

* Characteristic parameters of Logic families:
  1. Time propagation delay
  2. Power dissipation
  3. Figure of merit (FOM)
  4. Fan in
  5. Fan out
6) Noise Margin
7) High Logic

1) Time Propagation Delay:

It is the delay offered by per logic gate normally measured in nanoseconds.

\[ A \rightarrow 0 \rightarrow 1 \rightarrow \neg A \]

Delay is offered in the logic gate during the transition from high to low or low to high.

The fastest logic family is ECL, HTL is slowest.
2. **Power Dissipation**:
   - Power expenditure inside the logic gate to produce output.
   - CMOS has minimum power dissipation.
   - ECL has maximum power dissipation.

3. **Figure of Merit (FOM)**:
   - \[
   \text{Figure of Merit} = \frac{\text{Power dissipation}}{\text{Delay} \times \text{Power dissipation}}
   \]
   - Unit: Pico Joule.

   - Figure of merit must be as low as possible.
   - ISL has best figure of merit.
   - HTL has worst figure of merit.

4. **Fan In**:
   - Maximum number of inputs that can be applied to a logic gate.

5. **Fan Out**:
   - Diagram showing a logic gate with multiple inputs and outputs.
The output of one logic gate can be applied as input to the maximum no. of logic gate of same type is called as fan out.

CMOS : Maximum Fan Out
RTL  : Minimum Fan Out.

6) Wired Logic :

```
    O       O
   |       |
   |       |
   O       O
```

But

```
    O
   |  
```

The output of two logic gate are joint at a point that point will behave as either OR-gate or AND-gate.

Only ECL behave as wired-OR rest all other logic behave as wired-AND.

7) Noise Margin :

Maximum amount of noise added at the input so that it should not affect the output is called 'Noise Margin'.

HTL ⇒ Best Noise Margin,
RTL ⇒ Worst Noise Margin
Q. Identify the logic gate.

\[ V_{cc} \]

\[ R_A \quad R_B \]

\[ A \rightarrow B \rightarrow V_0 \]

\[ A \rightarrow \neg A = \text{Not gate.} \]

Q. Identify the logic gate.

\[ A \rightarrow \neg A = \text{Not gate.} \]
2. Identify the logic gate

(A + B) = A + B (Not)

A · B = X

A · B (AND Gate)
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<thead>
<tr>
<th>Parameters</th>
<th>RTL/DTL</th>
<th>I^2L</th>
<th>DTL</th>
<th>HTL</th>
<th>TTL</th>
<th>ECL</th>
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<td>Delay</td>
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<td>Power Dissipation</td>
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<td>FOM</td>
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<tr>
<td>Fan out</td>
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<tr>
<td>Noise Margin</td>
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<tr>
<td>Hired Logic</td>
<td></td>
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<tr>
<td>Basic gate</td>
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</tbody>
</table>
Oscillators

Those circuits which produce sustained oscillations are called as oscillators.

\[ V_o = AV_i \]

\[ \frac{V_o}{V_{in}} = A \]

\[ V_o = AV_i \]

\[ \beta V_i \]

\[ A \]

In an oscillator always true feedback is used.
Oscillator works without any external applied input.
Any disturbance (Noise) at the input may produce sustained oscillation.
Only if $|\alpha| = 1$ is also called Barkhawen Criteria.

* R-C Phase Shift Oscillator:

The output of the common emitter configuration produces the phase shift of 180°; the additional 3 R-C stages are used to provide a phase shift of additional 180° so that overall phase shift becomes 360° (0°).
So each R-C stage will provide 60° phase shift.

**Expression for R-C phase shift:**

\[
F_0 = \frac{1}{2\pi RC \sqrt{6} + \frac{4RC}{R}}
\]

When we cannot use transistor then \( R_C = 0 \)

\[
F_0 = \frac{1}{2\pi RC \sqrt{6}}
\]

* Hein's Bridge Oscillator *

\[ A = 1 + \frac{R_1}{R_1} \]

\[ \frac{1}{3} A \geq 1 \]

\[ \frac{1}{3} (1 + \frac{R_1}{R_1}) \geq 1 \]
\[ \omega = \frac{1}{RC}, \quad f = \frac{1}{2\pi RC} \]

\[ f_0 = \frac{1}{2\pi RC} \]

\[ C = 0.01 \mu F \]
\[ R_1 = 1 \text{ k}\Omega \]
\[ f_0 = 300 \text{ Hz} \]

\[ R = \frac{1}{2\pi f_0 C} = \frac{1}{2\pi \times 300 \text{ Hz} \times 0.01 \mu F} \]

\[ = \frac{10^8}{300 \times 2\pi} = \frac{10^6}{6\pi} \]

\[ = \frac{530 \text{ k}\Omega}{5.3 \times 10^5 \Omega} \]

\[ R = 530 \text{ k}\Omega \]
\[ \frac{1}{3} n \geq 1 \]
\[ \frac{1}{3} \left( 1 + \frac{R_2}{R_1} \right) = 1 \quad \text{(Worst Case)} \]

\[ 1 + \frac{R_2}{R_1} = 3 \]
\[ \frac{R_2}{R_1} = 2 \]
\[ \frac{R_2}{12} = 2 \]
\[ R_2 = 24 \quad \text{Amp} \]

* Heartly Oscillator *
The output of C.E. configuration provides a phase shift of 180° additional phase shift if tank circuit is used so that it can provide a phase shift of 180°. To provide sustained oscillation.

\[ X_L = X_C \]
\[ \omega_L = \frac{1}{\omega_C} \]
\[ \omega^2 = \frac{1}{L_C} \]
\[ \omega = \frac{1}{\sqrt{LC}} \]
\[ f_0 = \frac{1}{2\pi \sqrt{LC}} \]
\[ f_0 = \frac{1}{2\pi \sqrt{L_{eq}C_{eq}}} \]
\[ f_0 = \frac{1}{2\pi \sqrt{L_{1}+L_{2}}C} \]
**Colpits Oscillator**

\[ f_0 = \frac{1}{2\pi \sqrt{LC}} \]

\[ f_0 = \frac{1}{2\pi \sqrt{\frac{1}{LC}}} \]

\[ f_0 = \frac{1}{2\pi \sqrt{\frac{1}{L_{eq}} + \frac{1}{C}}} \]

\[ f_0 = \frac{1}{2\pi \sqrt{\frac{1}{L_{eq}} + \frac{1}{C_{eq}}}} \]

\[ f_0 = \frac{1}{2\pi \sqrt{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)}} \]
<table>
<thead>
<tr>
<th>Circuit</th>
<th>Formula</th>
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<tr>
<td>RC Phase Shift</td>
<td>$f_0 = \frac{1}{2\pi RC \sqrt{1+Q^2 R^2}}$</td>
</tr>
<tr>
<td>Hein's Bridge</td>
<td>$f_0 = \frac{1}{2\pi RC}$</td>
</tr>
<tr>
<td>Hartley</td>
<td>$f_0 = \frac{1}{2\pi \sqrt{(L_1+L_2)C}}$</td>
</tr>
<tr>
<td>Colpitts</td>
<td>$f_0 = \frac{1}{2\pi \sqrt{(\frac{1}{C_1}+\frac{1}{C_2})\frac{1}{L}}}$</td>
</tr>
</tbody>
</table>

\[ w = \frac{1}{RC} \]

\[ T = \frac{1}{w} = RC \]

\[ T = RC \]

\[ R = \frac{1000}{5\mu F} = 2 \times 10^8 \approx 10^8 \Omega \]
\[ T = RC \]
\[ = 1 \text{k}\Omega \times 1 \mu F = 1 \times 10^{-3} = 1 \text{ mili\,second} \]

**Second Method**

\[ V = 15^\circ \]
\[ T = 1000 \]
\[ C = 5 \mu F \]
\[ R = 9 \]

\[ Q = CV \]
\[ Q = 5 \mu F \times 15^\circ \]
\[ = 75 \mu C \]

\[ Q = It \]
\[ i = \frac{Q}{t} = \frac{75 \mu C}{1000} = 75 \text{ m\,A} \]
\[ R = \frac{15^\circ \times 10^9}{75} = 2 \times 10^8 \text{ \Omega} \]
* Consenses Theorem:

\[ y = AB + BC + \overline{AC} \]
\[ y = AB + BC (A + \overline{A}) + \overline{AC} \]
\[ = AB + \overline{A} BC + \overline{A} C \]
\[ = AB [1 + C] + \overline{AC} [B + 1] \]
\[ \therefore y = AB + \overline{AC} \]

Steps:

1. Total no. of variable \( w \) use = 3
2. Every variable must be repeated twice.
3. Select to the term which one \( w \) is the complement of other which \( w \) are not.

\[ \therefore \text{Find the minimise expression} \quad y = AB + \overline{BC} + \overline{AC} \]

\[ \text{Soln} \]
\[ y = AB + \overline{BC} \]

\[ \therefore y = AB + BC + AC \]

\[ \text{Soln} \]
\[ y = BC + AC \]

\[ \therefore y = \overline{AB} + BC + \overline{AC} \]

\[ \text{Soln} \]
\[ y = \overline{AB} + AC \]
Q:\ \[ y = \overline{A} \bar{B} + \overline{A} \bar{C} + \bar{B} \bar{C} \]

\[ y = \overline{A} \bar{B} + \overline{A} \bar{C} \]

\[ y = (A + B)(B + C)(\bar{A} + C) \]

\[ y = (\bar{A} + B)(\bar{A} + C) \]

\[ y = (\bar{A} + B)(\bar{A} + C) \]

\[ y = (\bar{A} + B)(\bar{A} + C) \]

\[ y = (\bar{x} + \bar{y})(\bar{y} + \bar{z})(x + \bar{z}) \]

\[ y = (\bar{x} + \bar{y})(\bar{y} + \bar{z})(x + \bar{z}) \]

Q: The current gain in the transistor \( \beta = 100 \). What is the value of collector current \( I_C \)?

\[ I_C \]

Diagram of an electronic circuit with voltage sources and resistors.
\(-12 + (Ie + I_B) 3k + I_B 150k + V_{BE} + I_E 3k = 0\)

\((Ie + I_B) 3k + I_B 150k + (I_B + I_C) 3k = 11.3\)

\(I_c 3k + I_B 3k + I_B 150k + I_B 3k + I_C 3k = 11.3\)

\(I_c 6k + I_B 156k = 11.3\)

\(\beta I_B 6k + I_B 156k = 11.3\)

\(100 \times 6kI_B + 156k I_B = 11.3\)

\(75.6 I_B = 11.3\)

\(\frac{I_B}{75.6} = 0.014 \text{ m.A.}\)

\(I_c = \beta I_B\)

\(= 100 \times 0.014 \text{ m.A.}\)

\(= 1.4 \text{ m.A.}\)

**Q.** In order to measure a maximum of 1 V with a resolution of 1 millivolt using n-bit analog to digital converter determine n-bit?

\(\text{Resolution} = 1 \text{ m.V.}\)

\(V_y = 1 \text{ V}\)

\(\text{Reso} = \frac{V_y}{2^n - 1}\)

\(\Rightarrow 1 \text{ m.V.} = \frac{1}{2^n - 1}\)

\(2^n - 1 = \frac{1}{1 \text{ m.V.}}\)
\[ 2^{11} - 1 = 1000 \]
\[ 2^n = 1001 \]
\[ 2^n \approx 2^{10} \]

\[ n = 10 \]

Q. A low pass filter formed by simple R-C circuit at the cut-off angular frequency. The voltage gain and the phase of output voltage relative to input voltage respectively, are:

(a) \(0.71, 45^{\circ}\)
(b) \(0.71, -90^{\circ}\)
(c) \(0.8, 90^{\circ}\)
(d) \(0.5, 90^{\circ}\)

\[ \frac{R}{C} \]

\[ V_i \]

\[ \frac{1}{j\omega C} \]

\[ V_o \]

\[ \text{low-pass filter} \]

\[ V_o = \frac{V_i \times \frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \]

\[ \frac{V_o}{V_i} = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega RC} \]

\[ \left| \frac{V_o}{V_i} \right| = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}} = \frac{1}{\sqrt{1 + (\omega RC)^2}} \]

\[ \left| \frac{V_o}{V_i} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega C}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega C}\right)^2}} \]
\[ w = w_0 \]
\[
\frac{V_o}{V_i} = \frac{1}{\sqrt{1 + 1}} = \frac{1}{\sqrt{2}} = 0.707
\]
\[
\frac{V_o}{V_i} = \frac{1}{1 + j\omega RC}
\]
\[
\angle \frac{V_o}{V_i} = -\tan^{-1}(\omega RC) = -\tan^{-1}\left(\frac{\omega}{\omega_c}\right)
\]
\[
= -\tan^{-1}\left(\frac{\omega}{\omega_c}\right) = -\tan^{-1}\left(\frac{\omega}{\omega}\right)
\]
\[
= -\tan^{-1}\left(\tan 45^\circ\right) = -\tan^{-1}\left(\tan 45^\circ\right)
\]
\[= -90^\circ \]

Ans

Digital Circuit Diagram
\[ x = 0, 1 \]

So, \[ x = 1 \]

\[ \overline{A} \overline{B} \overline{C} \cdot 1 + \overline{A} \overline{B} \overline{C} \cdot 1 + \overline{A} \overline{B} \overline{C} \cdot 1 + \overline{A} \overline{B} \overline{C} \cdot 1 = Z \]

\[ Z = \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} \overline{C} \]

\[ Z = \overline{A} \overline{B} + \overline{C} \]
$D_1 = \overline{Q_0}$

$D_0 = \overline{Q_2}$

$D_2 = \overline{Q_0 \overline{Q_1}}$

<table>
<thead>
<tr>
<th>$D_0$</th>
<th>$D_1$</th>
<th>$D_2$</th>
<th>$Q_0$</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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</tbody>
</table>
$x = 0, y = 0$ invalid

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>00</th>
<th>01</th>
<th>11</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
</tr>
</tbody>
</table>

$y = C \bar{A}$

Q. Identify the flip-flop.

$T = a \oplus \bar{q}$

so $a = D$
2. Identify

T-Flip-flop

\[ A \quad B \quad AB \quad C \quad D \quad CB \]

\[ A \quad B \quad C \quad D \]

8 min. no. of NAND gate required = 8.
* Flip-Flop Conversion:

Steps:
1. Identify the flip-flop which is required.
2. Draw the characteristic table.
4. Implement by logic gates.

(a) Convert $JK$ to $T$-flip-flop:

<table>
<thead>
<tr>
<th>$T$</th>
<th>$Q_n$</th>
<th>$Q_{n+1}$</th>
<th>$JK$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 X</td>
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<td>0</td>
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<td>1</td>
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<td>0</td>
<td>X</td>
</tr>
</tbody>
</table>

For $JK$ flip-flop:

$J = T$

$K = T$
* Convert JK to D flip-flop:

<table>
<thead>
<tr>
<th>D</th>
<th>Qn</th>
<th>Qn+1</th>
<th>JK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 X</td>
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<td>1</td>
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<td>X 1</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>X 0</td>
</tr>
</tbody>
</table>

\[ J = D \]
\[ K = \overline{D} \]
* Convert D to T flip-flop:

<table>
<thead>
<tr>
<th>T</th>
<th>( q_n )</th>
<th>( q_{n+1} )</th>
<th>D (( = q_{n+1} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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</table>

\[ D = \overline{T} q_n + T \overline{q}_n \]

\[ D = T \oplus q_n \]

\[ T = D \oplus q_n \]
* Point to be remembered:

\[ JK \rightarrow T \]
\[ J = D \]
\[ K = \overline{D} \]
\[ D \rightarrow \top \]
\[ D = T \oplus \emptyset \]
\[ \top \rightarrow D \]
\[ T = D \oplus \emptyset \]

\[ SR \rightarrow D \]
\[ S = D \]
\[ K = \overline{D} \]
Steps for Identification

1. Draw the circuit diagram by using ordinary gate.
2. Substitute bubble in front of AND gate and input of OR gate so that bubble is balanced.
3. Replace every gate by Nand gate, it gives minimum no. of nand gate.

Ex -

\[
\begin{align*}
A \quad & \quad A \cdot B \\
B \quad & \quad AB + C \cdot D \\
C \quad & \quad CD \\
D \quad & \quad \\
\end{align*}
\]

\[
\begin{align*}
A \quad & \quad A \cdot B \\
B \quad & \quad \quad \quad C \cdot D \\
C \quad & \quad D \\
D \quad & \quad \\
\end{align*}
\]

\[
y = AB + CD + E
\]
\[ y = A \bar{B} + C \bar{D} + E \]
Steps for identification minimum no. of Nor gate:

1. Draw the circuit diagram by using ordinary gates.

2. Substitute bubble at the infront of OR-gate and at the input of AND-gate.

3. Replace every gate by NOR-gate it will give minimum no. of nor gate.
\[ y = \overline{A} + \overline{B} \]

Duality -
\[ \overline{A + B} \]

OR

OR- Gate

\[ f(A, B, C, D, E) = C + \overline{D} E \]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
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\[ = \Phi \]
model Gunter

4 = 2^2 = 16
For the given circuit diagram, identify the mod. $\text{mod } 10$. 
Draw the circuit diagram for mod-12 up counter using all given inputs.

\[ f(A, B, C, D) = AC + ABD + ACD. \]
The image contains a hand-drawn table and a tree diagram. The table has columns labeled $I_0, I_1, I_2, I_3, I_4, I_5$ and rows labeled $B_0, B_1, B_2, B_3$. The values in the table are:

- $B_0$: 1
- $B_1$: 0
- $B_2$: 1
- $B_3$: 0

Below the table, there is a tree diagram with nodes labeled $f_A$, $1111$, $1010$, $0000$, $0101$, $1$, and $0110$. The tree diagram shows a path leading to the node $0110$.

At the bottom of the page, there are calculations:

- $1011 - 1001 = 0100$
- $6 + (-5) = 1$
- $0001$

The calculations and tree diagram suggest a process involving binary values and arithmetic operations.
\( FE )_H \oplus S_F H

0 1 1 1 1 1 1 1 1
+ 0 1 0 1 1 1 1 1 1
\[ 0 0 1 0 0 0 0 1 \]
\[ \text{exor} \]

\[ \begin{array}{c}
0 0 0 0 0 0 0 0 0 \\
0 0 0 0 0 0 0 0 0 \\
0 0 0 0 0 0 0 0 1 \\
0 0 0 0 0 0 0 1 1
\end{array} \]

\[ \begin{array}{c}
0 0 1 0 0 1 0 1 1
\end{array} \]

\[ \begin{array}{c}
\hline
D_3 \\
D_2 \\
D_1 \\
D_0 \\
S, S_0
\end{array} \]

\[ \begin{align*}
\overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} + A \overline{B} &+ \overline{A} B \\
\overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} + A \overline{B} &+ \overline{A} B + \overline{B} C \\
\overline{A} [B + \overline{B} C] &+ A [B + \overline{B}] \\
\overline{A} [B + C] &+ A \\
\overline{A} B + \overline{A} C &+ A \\
\overline{A} B + \overline{A} C &+ A \\
\overline{A} B + A + C &+ A \\
A + B + C
\end{align*} \]
\[
\begin{array}{c}
QR 00 01 11 10 \\
0 1 1 1 \\
1 1 1 1 \\
\hline
4 3 7 6
\end{array}
\]

\[= \overline{P}R + PR + Q\]

\[= P + R + Q\]

one xor and 1 or

38. 15-bit

39.

\[10011\]

\[\overline{1100}\text{ 1's}\]

\[\overline{1101}\text{ 2's}\]

\[\overline{-13}\]

40.

\[D J K 1\]

\[E 1\]

\[B J K 1\]

\[A J 1\]
Series RLC Network:

\[ Z = R + j\omega L + \frac{1}{j\omega C} \]
\[ = R + j\omega L - \frac{1}{j\omega C} \]
\[ = R + j\left(\omega L - \frac{1}{\omega C}\right) \]
\[ |Z| = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \]

At resonance:
\[ \omega L = \frac{1}{\omega C} \]

\[ Z = \sqrt{R^2} \]
\[ Z_{\min} \approx R_{\min} \]

\[ I = \frac{V}{Z} \]
\[ I = \frac{V}{R_{\min}} \text{ (maximum)} \]

\( I_{\text{max}} \) at resonance freq.
Use of Resonance:

It is used to select only a single frequency by neglecting all other frequencies.

Loud Speaker:

\[
Z = \sqrt{R^2 + (\omega_c - \omega)^2}
\]

To calculate the resonance freq. of any circuit, equate imaginary component of expression to zero.
2. For the given circuit diagram determine the resonance frequency.

\[
Z_1 = \frac{1}{\omega C}
\]

\[
\text{So } Z = Z_1 + \frac{1}{j\omega C} = \frac{j\omega + \frac{1}{j\omega}}{1 + j\omega}
\]

\[
= \frac{1 + j\omega - \omega^2}{j\omega (1 + j\omega)}
\]

\[
= \frac{-j(1 - \omega^2) + j\omega}{\omega (1 + j\omega)}
\]

\[
= \frac{-j(1 - \omega^2) + j\omega (1 - j\omega)}{\omega (1 + j\omega) (1 - j\omega)}
\]

\[
= \frac{-j[(1 - \omega^2) + j\omega - j\omega (1 - \omega^2) + \omega^2]}{\omega (1 + \omega^2)}
\]
\[-J(1-w^2) + \omega - \omega(1-w^2)r jw^2 \]
\[= \frac{-\omega(1-w^2) - j[\sqrt{1-w^2} + jw^2]}{\omega(1+w^2)} \]
\[= \frac{\omega - \omega(1-w^2) - j}{\omega(1+w^2)} \]
\[= \frac{\omega - \omega(1-w^2)}{\omega(1+w^2)} \quad - \frac{j}{\omega(1+w^2)} \]

So \(-1 = 0\) not possible

So resonant freq. does not exist.

For the given circuit diagram calculate given frequency. (Resonance).

For simplicity

Conductance \(= \sqrt{jwC + \frac{1}{R+j\omega L}} \)
\[
\frac{jwC (R + jwL) + 1}{(R + jwL)(R - jwL)}
\]

\[
\begin{align*}
&= \frac{jwL}{R^2 + \omega^2 L^2} \\
&= \frac{jwRC [R + j\omega] + R + \omega^2 LC (1 + j\omega)\omega}{(R^2 + \omega^2 L^2)} \\
&= \frac{jwRC - \omega^2 RC + R + \omega^2 RC + j\omega^2 LC - j\omega}{R^2 + (\omega L)^2}
\end{align*}
\]

Equating imaginary part to zero,

\[
y \left( \frac{\omega RC + \omega^2 LC - \omega L}{R^2 + (\omega L)^2} \right) = 0
\]

\[
\frac{R^2 C + \omega^2 LC - L}{R^2 + (\omega L)^2} = 0
\]

\[
R^2 C + \omega^2 LC - L = 0
\]

\[
\omega^2 L^2 C = L - R^2 C
\]

\[
\omega^2 = \frac{L - R^2 C}{R^2 C} - \frac{R^2}{L^2 C}
\]

\[
\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2 C}}
\]
Q. Calculate the resonance frequency.

\[ \omega = \frac{1}{\sqrt{L C}} = \frac{1}{\sqrt{2 \times 10^{-3} \times 0.25}} = 1.73 \]

but it is not right.

\[ \omega = \sqrt{\frac{1}{LC} - \frac{R^2}{c^2}} \]
\[ D + T + H \]

\[ D \rightarrow 1 \quad \text{if} \quad T \text{ or } H \]

\[ T \rightarrow 1 \quad \text{if} \quad H \text{ or } T \]

\[ D = 1 \quad \text{on the clock} \]

\[ D \text{ or } T \text{ and humidity} \]

\[ \text{if} \quad 1 \quad 1 \quad 1 \quad \rightarrow A \cdot 0 \]

\[ D + T . H \]
*Half-Wave Rectifier:*

Step-up transformers increase the amplitude of applied i/p and reproduces at secondary of the transformer.

If the applied i/p whose amplitude is decrease, it called as step down transformer.

*P.e. Value or Average value:*

\[ V_{avg} = \frac{1}{2\pi} \int_{0}^{2\pi} f(t) \, dt \]

\[ = \frac{1}{2\pi} \int_{0}^{2\pi} V_m \sin \theta \, d\theta \]
\[ \frac{1}{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} V_m \sin \theta \, d\theta + \frac{1}{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} 0 \, d\theta = \frac{V_m}{\frac{\pi}{2}} \left[ \cos \theta \right]_0^{\frac{\pi}{2}} = \frac{V_m}{\frac{\pi}{2}} \]

So Average value of half wave rectifier \( = \frac{V_m}{R} \)

# Average value of Full wave Rectifiers:

dc value

\[ \frac{2V_m}{\sqrt{2}} \]

* Root mean square value:

Power is also called as mean square value of function.

\[ \sqrt{\frac{1}{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} f(\theta)^2 \, d\theta} \]

\[ \sqrt{\frac{1}{\frac{\pi}{2}} \left[ \int_0^{\frac{\pi}{2}} f(\theta) \, d\theta \int_0^{\frac{\pi}{2}} f(\theta)^2 \, d\theta \right]} \]

\[ = \sqrt{\frac{1}{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} (V_m \sin \theta)^2 \, d\theta} \]

\[ = \sqrt{\frac{1}{\frac{\pi}{2}} \int_0^{\frac{\pi}{2}} V_m^2 \sin^2 \theta \, d\theta} \]
\[ V_m \sqrt{\frac{1}{\pi} \int_0^{\infty} \sin^2 \theta d\theta} \]

\[ = \frac{V_m}{\alpha} \sqrt{\frac{1}{\pi} \int_0^{\infty} \left( 1 - \frac{\sin^2 \theta}{2} \right) d\theta} \]

\[ = \frac{V_m}{\alpha} \sqrt{\frac{1}{\pi} \left( \frac{\pi}{2} \right)} \]

\[ = \frac{V_m}{\alpha} \]

H. H. R. \quad V_{rms} = \frac{V_m}{\alpha} \]

F. H. R. \quad V_{rms} = V_m \sqrt{2} \]

H. H.

\[ 2.8 \]

\[ V_{ave} = \frac{V_m}{\alpha} = \frac{V}{X} \]

\[ I_{ave} = \frac{4}{\pi X/10} \]

\[ I_{ave} = 0.9 \frac{V}{X} \]
**Full Wave Rectifier**: 

\[ V_m = 10 \]

\[ V_{ave} = \frac{2V_m}{\pi} \]

\[ = \frac{20}{\pi} \]

\[ I_{av} = \frac{V_{ave}}{R} = \frac{20}{R} = \frac{20}{\mu A} \]

\[ R_L = 2K \]

\[ 10V \]
* Thevenin’s Theorem:

\[ V_{th} = \text{Open circuit voltage} = V_{oc}. \]

For thevenin’s resistance \( R_{th} \):

To calculate thevenin’s resistance and short the voltage source and open the current source.
2. For the given circuit diagram, calculate the Thevenin's voltage and Thevenin's resistance.

Solution:

Loop 1:
\[ I_1 \times 2 \Omega + V_{th} - I_2 \times 3 \Omega = 0 \]

\[ V_{th} = I_2 \times 3 \Omega - I_1 \times 2 \Omega \]

\[ V_{th} = 2 \times 3 - 2 \times 2 = 6 - 4 = 2 \text{ V} \]

Loop 2:
\[ -V_{th} + I_1 \times 3 \Omega - I_2 \times 2 \Omega = 0 \]

\[ V_{th} = V_1 \times 3 \Omega - I_2 \times 2 \Omega \]

\[ V_{th} = 2 \text{ V} \]
To calculate thevenin's resistance:

\[ R_{th} = \frac{3 \times 8}{3 + 2} + \frac{3 \times 2}{3 + 2} \]

\[ = \frac{6}{5} + \frac{6}{5} \]

\[ R_{th} = \frac{12 \cdot 5}{5} \]
\[ -20 + j \times 2k + j \times 2y + 10 = 0 \]

\[ I \times jk = 10 \]

\[ I = 9.5 \text{ mA} \]

\[ V_{10} + j \times 2k + 10 = 0 \]

\[ V_{10} = 10 + j \times 2k \]

\[ 10 + 5 = 15 \text{ V} \]

\[ R_{\text{th}} = \frac{2 \times 2}{9 + 2} = \frac{4}{11} \]

\[ R_{\text{th}} = 1\Omega \]

**Q.** For the given circuit diagram calculate Thévenin voltage and Thévenin resistance.
\[ \begin{align*}
-10 I_2 \cdot 2k + I_2 \cdot 2k &= 0 \\
I_2 &= \frac{10}{4k} = 2.5 \text{ mA} \\
-20 + I_1 \cdot 2k + I_1 \cdot 2k &= 0 \\
I_1 &= \frac{20}{4 \cdot 1k} = 5 \text{ mA} \\
V_{th} + I_2 \cdot 2k - 2k \cdot I_1 &= 0 \\
V_{th} &= 2k \cdot I_1 - I_2 \cdot 2k \\
&= 2k \cdot 5 - 2.5 \times 2 \\
&= 10 - 5 \\
V_{th} &= 5 \text{ V} \\
\end{align*} \]

For \( R_{TH} \):

\[ R_{TH} = 2k \]
\( \text{find } v \text{ b/w a \& b.} \)

\[ \frac{2 V}{2 \Omega} = \frac{2 V}{2 \Omega} \]

\[ \text{Replace: ideal } \]

\[ \text{it is a Wheatstone Bridge. So current flow through galvane} \]

\[ \text{meter is 0 so no current flow through it.} \]

\[ \begin{align*}
\text{for } I_1 &= \frac{q}{V} = 0.5 \text{ mA} \\
\text{for } I_2 &= 0.5 \text{ mA}
\end{align*} \]
\[
-38 + I_1 \times 5 + (I_1 - I_2) \times 9 = 0 \\
9I_1 - 9I_2 = 88 \quad \text{①} \times 6 \\
+76 + 2I_2 + 9(I_2 - I_1) = 0 \\
-9I_1 + 6I_2 = -76 \\
9I_2 - 6I_1 = 76 \quad \text{②} \times 9 \\
54I_1 - 24I_2 = 88 \times 6 \\
16I_1 - 24I_2 = 96 \times 4 = 384 \\
-98I_1 = 38 \times 6 - 76 \times 9 \\
\begin{align*}
\begin{cases}
I_1 = 2 \\
I_2 = -16
\end{cases}
\end{align*}
\]

Hence $9 \times 2 + 38 = 58$ 

$\frac{58}{2} = 29$
\[-3\theta + 5 i_1 + V_{th} = 0\]
\[V_{th} = -5 i_1 + 3\theta\]
\[= -5 \times \frac{38}{5} - 38\]
\[= 5 \times 38 + 7 \times 38\]
\[\frac{7}{7}\]
\[V_{th} = 6.5 \, V\]

\[-V_{th} + 2 i_1 + 76 = 0\]
\[-V_{th} = -76 - 2 i_1\]
\[V_{th} = 76 + 2 \times (-38)\]
\[V_{th} = 76 - \frac{76}{7}\]
\[V_{th} = 6.5 \, V\]

\[\overline{Q.34}\]

\[\text{Clamper}\]

\[+ V_{in} + V_{in} - V_{out} = 0\]

\[V_{out} = 2 \, V_{in}\]
\(-10 + IR = 0\)

\[ R = \frac{10}{I} \]
\[ R = \frac{10}{10} = 1 \]

\[ R = 1 \text{ k}\Omega \]

When Zener diode, it is in the R.B. state.

\[ V \]
\[ I \]
\[
\frac{O/P}{I/P} = \text{gain}
\]

\[20 \log \left( \frac{O/P}{I\text{m.V.}} \right) = -80 \text{dB}.\]

\[
\log \left( \frac{O/P}{I/P} \right) = \frac{-50}{2.5} = -2.5
\]

\[
O/P = 1 \text{ m.V} \times 10^{-2.5}
\]
When no input is applied some output voltage is achieved called output offset voltage \((V_{oo})\).

\[
\begin{align*}
\text{To cancel the output offset voltage some input } & \text{ is applied in non-inverting terminal } V_i \text{ called as input offset voltage } (V_{io}) \text{.}
\end{align*}
\]

\[
\begin{align*}
\frac{V_{oo}}{V_i} &= \left(1 + \frac{R_6}{R_i}\right) \\
V_{oo} &= V_i \left(1 + \frac{R_6}{R_i}\right)
\end{align*}
\]
\[ \frac{V_b}{V_i} = A = \frac{V_o}{V_d} \]

\[ V_o = A_d V_d \]

\( A_d \): differential gain

\( V_d \): differential input voltage

Example:

The ideal value of CMRR is must be \( \infty \).

\[ V_o = A_d V_d + A_c V_c - \frac{V_1 + V_2}{2} \]

\[ \text{CMRR} = \frac{A_d}{A_c} = \infty \]

For the given output voltage relation calculate CMRR.

\[ V_o = 10 \left( V_2 - V_1 \right) \text{ rad} \]

\[ V_o = A_d V_d + A_c V_c \]

\[ \text{CMRR} = \frac{A_d}{A_c} = \frac{10}{0} = \infty \]
For the given circuit diagram calculate CMRR, \[ V_0 = A_d V_d + A_c V_c \]

\[ V_{in} = \frac{V_2 R_2}{R_1 + R_2} = \frac{V_2 X + K}{4 + 2} = \frac{9 V_2}{6} = \frac{3}{2} V_2 \]

\[ i_1 + i_e = 0 \]

\[ \frac{V_1 - V_{in}}{+} + \frac{V_0 - V_{in}}{-} = 0 \]

\[ \frac{V_0 - V_{in}}{\pm} = \pm (V_1 - V_2) = V_{in} - V_1 \]

\[ V_0 - V_{in} = 2.5 V_{in} - 2.5 V_1 \]

\[ V_0 = 3.5 V_{in} - 2.5 V_1 \]

\[ V_0 = \frac{3.5}{2} V_2 - \frac{5}{2} V_1 \]

\[ V_c = \frac{V_0 + V_1}{2} \Rightarrow 2 V_c = V_1 + V_2 \quad \text{(10)} \]

\[ V_d = V_2 - V_1 \Rightarrow V_d = V_2 - V_1 \quad \text{(11)} \]

\[ V_2 = V_c + \frac{V_{in}}{2} \quad \text{(11)} \]

\[ 2 V_c + V_d = 2 V_2 \]
\( 2V_c = V_1 + \sqrt{2} \)

\( V_d = \sqrt{2} - V_1 \)

\( 2V_c - V_d = 2V_1 \)

\[
V_1 = V_c - \frac{V_d}{2}
\]

\( V_0 = \frac{7}{6} V_c - \frac{5}{2} V_1 \)

\( V_0 = \frac{7}{6} \left( V_c - \frac{V_d}{2} \right) - \frac{5}{2} \left( \frac{V_c - V_d}{2} \right) \)

\( V_0 = \sqrt{V_c} \left( \frac{7}{6} \right) \)

\( V_0 = \left( \frac{7}{6} V_d - \frac{5}{4} V_1 \right) + \left( \frac{7}{6} V_c - \frac{5}{2} V_c \right) \)

\( V_0 = V_d \left( \frac{7}{6} + \frac{5}{4} \right) + V_c \left( \frac{7}{6} - \frac{5}{2} \right) \)

\( V_0 = V_d \left( \frac{29}{12} \right) + V_c \left( -\frac{1}{6} \right) \)

\( CMRR = \frac{A_d}{A_c} = \frac{\frac{29}{12}}{-\frac{1}{6}} = -\frac{29}{2} \)

\( = -14.5 \)

**Q. Determine CMRR of given circuit:**

![Circuit Diagram](image)
\[ V_{an} = \frac{V_2 \times 3K}{3K+1K} = \frac{3V_2}{4} \]

\[ \frac{V_0 - V_{an}}{10K} + \frac{V_1 - V_{an}}{2K} = 0 \]

\[ \frac{V_0 - 3V_2}{\frac{9}{4}} + \frac{V_1 - 3V_2}{2K} = 0 \]

\[ V_0 = -5V_1 + \frac{15V_2}{9} + \frac{9V_2}{4} \]

\[ V_0 = -5V_1 + \frac{9}{2}V_2 \]

\[ V_c = \frac{V_1 + V_2}{2} \]

\[ V_1 = V_c - \frac{V_d}{2} \]

\[ V_2 = V_c + \frac{V_d}{2} \]

\[ V_0 = -5V_c + 9.5V_c + \left( \frac{5V_d}{2} + \frac{9}{4}V_d \right) \]

\[ V_0 = -0.5V_c + \frac{19}{4}V_d \]

\[ CMRR = \frac{M_d}{M_c} = \frac{19.4}{-1.4} = \frac{19}{-2} \]

\[ CMRR = \frac{19}{-2} \]
\[ A_d = 200 \text{dB} \]

\[ \text{CMRR} = 80 \text{dB} \]

\[ \text{CMRR} = \left| \frac{A_d}{A_c} \right| \]

\[ \text{CMRR} = 20 \log \left| \frac{A_d}{A_c} \right| = 86.7 \]

\[ \Rightarrow \log \left| \frac{A_d}{A_c} \right| = 4 \]

\[ \Rightarrow A_d = 10^4 A_c \]

\[ 200000 = 10^4 A_c \]

\[ A_c = \frac{200000}{10^4} \]

\[ A_c = 20 \]

\[ \text{gain} = \frac{V_o}{V_{in}} = \frac{1500}{15} = 100 \]

\[ 20 \log 100 = 40 \]

\[ A_{dB} = 10 \log \frac{P_o}{P_{in}} \]

\[ = 10 \log \frac{V_o^2}{V_{in}^2} = 86.7 \text{dB} \]
\[ R = \frac{R_o}{I_{in}} = \frac{1500}{1.5} = 1000 \]

\[ A_{dB} = 10 \log 1000 = 90 \text{ dB} \]

\[ \text{Ans} = 0.2 \text{ V} \]
<table>
<thead>
<tr>
<th>$\frac{I_C}{I_E} \leq 1$</th>
<th>$A &gt; 1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_V = \frac{V_{CE}}{V_{BE}} &gt; 1$</td>
<td>$A_V = \frac{V_{CE}}{V_{BE}} \approx 1$</td>
</tr>
<tr>
<td>high</td>
<td>low</td>
</tr>
<tr>
<td>low</td>
<td>high</td>
</tr>
</tbody>
</table>

$V_{CE} - V_{BE} - V_{CB} = 0$

$V_{CE} \approx V_{CB}$

halfwave rectifies

$$\Sigma I = \sqrt{\frac{I_{rms}^2}{I_{dc}^2}} - 1$$

$$\gamma = \sqrt{\frac{1}{\frac{m}{L} + \frac{1}{R_c R}} - 1}$$

$$\gamma = \sqrt{\frac{m}{L} - 1}$$

$$\gamma = \sqrt{1.2} \sum A$$
Full wave rectifier:

\[ \phi = \sqrt{\frac{I_{\text{rms}}}{I_{\text{dc}}}} \cdot 1 \]

\[ = \sqrt{\frac{\frac{I_{\text{rms}}^2}{\alpha^2}}{\left(\frac{E_{\text{rms}}}{\alpha x}\right)^2}} - 1 \]

\[ = \sqrt{\frac{1}{\alpha^2}} - 1 \]

\[ = \sqrt{\frac{x^2}{\alpha}} - 1 \]

\[ \approx 0.46 \]

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Those group of frequencies where gain is approximately constant is called as B.I.D.
8.11: Upper cut off frequency
\[ f_c - 0 = f_c \]

Low cut off frequency

High pass filter:

\[ B_1 = \infty - 0 = \infty \]

Bandpass filter:

\[ B_1 = f_{c_2} - f_{c_1} \]

Band rejection filter:

\[ B_2 = \infty - 0 \]

\[ B_2 = \infty \]
Gain \times Bandwidth product always decreases.

\[ A \times f_b, = \text{constant} \]

\[ A \times f_c, = \text{constant} \]

Gain = \frac{100}{1 + 100 \times 0.899} = \frac{100}{1 + 100 \times 0.899} = \frac{100}{100} = 10

So gain will decrease by 100 times.
Gain: $\dfrac{6H \times (1 + 10\beta)}{100 \times (1 + 100 \times 0.099)}$ 

$= \dfrac{600 \times (1 + 9)}{100}$

$\beta = 0.1$

$A_{CL} = \dfrac{A}{1 - 10\beta}$

Output: $P_{in} \times (1 - 10\beta)$

Output $= 700 \times [S1]$

Output $= 10200 \times k$

7.8

Second Method
for any LC circuit cut-off freq. is given by resonance. freq.

\[ f = \frac{1}{\sqrt{LC}} \]

\[ \omega = \frac{1}{\sqrt{LC}} \]